AF/IEW $

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop Appeal Brief –Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

June 5, 2007
Date

Sherri A. Phillips

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/773,583	Confirmation No.	: 6732
Applicants	: Douglas A. Larson and Jeffrey J. Cronin		
Filed	: February 5, 2004	Attorney Docket No.:	501296.01 (30266/US)
Art Unit	: 2188	Customer No.	: 27,076
Examiner	: Duc T. Doan		
Title	: APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM		

APPEAL BRIEF TRANSMITTAL

Mail Stop Appeal Brief –Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith, in triplicate, is the Appeal Brief in this application, with respect to the Notice of Appeal filed on April 5, 2007 A check in the amount of $500.00 is also enclosed to cover the fee for filing the Appeal Brief.

Any deficiency or overpayment should be charged or credited to Deposit Account No. 50-1266. This transmittal is being submitted in duplicate.

Respectfully submitted,

DORSEY & WHITNEY LLP

Karen Lenaburg
Registration No. 58,371

KL:sp

Enclosures:
Postcard
Check
Appeal Brief (+ 2 copies)
Copy of this Transmittal

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
Tel: (206) 903-8800
Fax: (206) 903-8820

Effective on 12/08/04

FEE TRANSMITTAL SHEET (FY 2006)

Complete if Known	
Application No.	10/773,583
Filing Date	February 5, 2004
First Inventor	Douglas A. Larson
Group Art Unit	2188
Examiner Name	Duc T. Doan
Atty. Docket Number	501296.01 (30266/US)

[ ] Applicant claims small entity status (see 37 C.F.R. 1.27)

METHOD OF PAYMENT (Check One)

[X] The Director is hereby authorized to charge any additional fee required under 37 C.F.R. §§ 1.16 and 1.17 and 1.136(a)(3) and credit any over payments to Deposit Account No. **50-1266;** Deposit Account Name: **DORSEY & WHITNEY LLP.**

[X] Check Enclosed.

Extra Claim Fees

Current Claims		Prior		Extra		Fee		Fee Paid
Total	4	- 43	=	0	x	$50	=	$ 0
Ind.	1	- 9	=	0	x	$200	=	$ 0
Multiple Dependent Claims					x	$360	=	$0
						Subtotal (Extra Claims)		$ 0

Petition Fee Under 37 CFR 1.17(f), (g), & (h)

Enclosed is a Petition filed under 37 CFR as indicated below:

[ ] Petition Fee under 37 CFR 1.17(f) **Fee $400**

§ 1.53(e)	to accord a filing date.
§ 1.57(a)	to accord a filing date.
§ 1.182	for decision on a question not provided for.
§ 1.183	to suspend the rules.
§ 1.378(e)	for reconsideration of decision on petition refusing delayed payment of maintenance fee in expired patent.
§ 1.174(b)	to accord a filing date to an application under §1.740 for extension of patent term.

[ ] Petition Fee under 37 CFR 1.17(g) **Fee $200**

§ 1.12	**for access to an assignment record.**
§ 1.14	**for access to an application.**
§ 1.47	**for filing by other than all inventors or person not the inventor.**
§ 1.59	**for expungement of information.**
§ 1.103(a)	**to suspend action in an application.**
§ 1.136(b)	**for review of a request for ext. of time when** §1.136(a) not avail.
§ 1.295	for review of refusal to publish a statutory invention registration.
§ 1.296	to withdraw a req. for pub. after notice of intent to publish issued.
§ 1.377	for review of decision refusing to accept a maintenance fee filed prior to expiration of a patent.
§ 1.550(c)	**for request for ext. of time in** *ex parte* reexam. proceedings.
§ 1.956	**for request for ext. of time in** *ex parte* reexam. proceedings.
§ 5.12	for expedited handling of foreign filing license.
§ 5.15	for changing the scope of a license.
§ 1.5.25	for retroactive license.

[ ] Petition Fee under 37 CFR 1.17(h) **Fee $130**

§ 1.19(g)	to request documents in a form other than provided in this part.
§ 1.84	for accepting color drawings or photographs.
§ 1.91	for entry of a model or exhibit.
§ 1.102(d)	to make an application special.
§ 1.138(c)	to expressly abandon an application to avoid publication.
§ 1.313	to withdraw an application from issue.
§ 1.314	to defer issuance of a patent.

FEE CALCULATION (Continued)

3. ADDITIONAL FEES

Large Entity Fee	Small Entity Fee	Fee Description	Fee paid
50	25	Surcharge - late provisional filing fee or cover sheet	$
130	65	Surcharge – Late nonprovisional filing fee or oath	$
180	180	Submission of IDS	$
40	40	Recording each patent assignment per property (times number of properties)	$
120	60	Extension for reply within first month	$
450	225	Extension for reply within second month	$
1,020	510	Extension for reply within third month	$
1,590	795	Extension for reply within fourth month	$
2,160	1,080	Extension for reply within fifth month	$
790	395	Submission After Final 1.129	$
500	250	Notice of Appeal	$
500	250	Filing a brief in support of an appeal	$500
1,000	500	Request for oral hearing	$
130	65	Terminal Disclaimer Fee	$
800	400	Design Issue Fee	$
790	395	Request for Continued Examination (RCE)	$
130		Request for voluntary publication or republication	$
500	250	Petition to Revive – unavoidable	$
1,500	750	Petition to Revive – unintentional	$
200		Filing for patent term adjustment	$
400		Request for reinstatement of term reduced	$
1,120		Extension of term of patent	$
OTHER FEE (specify)			$
		Subtotal (Additional Fees)	$0
		Total Amount of Payment:	**$500**

Submitted by:

CUSTOMER NUMBER	DORSEY & WHITNEY LLP	1420 Fifth Avenue, Suite 3400 Seattle, WA 98101-4010 (206) 903-8800 *phone* / (206) 903-8820 *fax*
27,076		

Name: Karen Lenaburg — Reg. No.: 58.371

Signature: Karen Lenaburg — Date: 6/5/07

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450. Alexandria, VA 22313-1450.

June 5, 2007
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Sherri A. Phillips

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF (37 C.F.R. § 41.37)

Sir:

This brief is in furtherance of the Notice of Appeal filed in this case on April 5, 2007. The fees required under Section 41.20, and any required request for extension of time for filing this brief and fees therefore, are dealt with in the accompanying transmittal letter.

06/07/2007 RFEKADU1 00000025 10773583
01 FC:1402 500.00 OP

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, Micron Technology, Inc., a Delaware Corporation having a principal place of business in Boise, Idaho.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to appellants, the Appellants' legal representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-43.

B. STATUS OF ALL THE CLAIMS

1. Claims canceled: 1-39.
2. Claims withdrawn from consideration but not canceled: None.
3. Claims objected to: None.
4. Claims allowed or confirmed: None.
5. Claims rejected: 36-43.

C. CLAIMS ON APPEAL

The claims on appeal are: 40-43.

IV. STATUS OF AMENDMENTS

Appellants canceled claims 1-4, 11-15, 21-25, and 32-39 after final rejection. (Response dated February 5, 2007 attached hereto as Exhibit B and the Supplemental Response dated June 5, 2007 attached hereto as Exhibit C).

V. SUMMARY OF CLAIMED SUBJECT MATTER

1. Introduction

The present application is directed toward solving the problem of data collisions on a bi-directional data bus in a memory system. In one embodiment shown in Figure 1, a memory system has multiple memory modules 130a-n connected to each other in series and to a memory hub controller 128 via a bi-directional data bus. Data collisions can occur on a bi-directional data bus when a read command is issued before a write command. For example, as read data is heading downstream from a memory device on memory module 130c and write data is simultaneously heading upstream from the memory hub controller 128 to memory module 130n, the read data and the write data would collide. The present application prevents this data collision by using a bypass circuit 286. In one embodiment, the bypass circuit 286 is capable of temporarily storing data passing through a respective memory hub 140. As in the example provided above, as the read data is about to head downstream toward memory module 130b from memory module 130c, the write data is heading upstream from memory module 130a toward memory module 130b. In order to prevent a data collision, the write data is temporarily stored in the bypass circuit 286 in the memory hub 140 of memory module 130b. While the write data is stored in the bypass circuit 286, the read data continues downstream to memory module 130a. Once the read data passes through memory module 130b on its way to memory module 130a, the write data may be recoupled to the bi-directional data bus to continue its way upstream to memory module 130n. Therefore, when a read command is issued before a write command, the corresponding write data can be sent upstream before the read latency of the previously issued read command is complete. *Specification,*. at page 8, lines 12-27, page 10, lines 21-28, page 11, lines 1-22 and Figure 3. (Specification attached hereto as Exhibit D).

2. Claim 40

Claim 40 is directed toward a method for executing read and write commands in a memory system having a bidirectional memory bus. *Specification,* at page 5, lines 15-17. The method of claim 40 includes "issuing a read command to access a first memory location in the memory system" and "before completion of the read command, scheduling a write command to

write data to a second memory location in the memory system." In one embodiment, a read command is issued by the memory hub controller 128 to access a first memory location in a memory system. Before completing the read command, a write command is scheduled by the memory hub controller 128 to write data to a second memory location in the memory system. *Id.* at page 10, lines 21-28.

In addition, claim 40 includes "retrieving read data from the first memory location." In one embodiment, the read data is retrieved from the first memory location. *Id.* at page 10, lines 21-28.

Claim 40 further includes "prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system." In one embodiment, prior to the memory hub controller 128 receiving the read data on the memory bus, the write data corresponding to the write command is provided to the bidirectional memory bus. *Id.* at page 10, lines 27-28 and page 11, line 1.

Claim 40 further includes "in the memory system, bypassing the read data on the bidirectional memory bus." In one embodiment, the read data on the bidirectional memory bus is bypassed while in the memory system when a bypass circuit 286 captures the write data so that read data can be sent to the memory hub controller 128. *Id.* at page 11, lines 1-14. Finally, claim 40 includes "receiving the read data on the bidirectional memory bus from the memory system" and "providing the write data to the bidirectional memory bus." In one embodiment, the read data on the bidirectional memory bus is received by the memory hub controller 128 from the memory system. *Id.* In addition, the write data is provided back to the bidirectional memory bus. *Id.*

VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

The only ground of rejection to be reviewed on appeal is whether claim 40, as well as any claims dependent thereon, are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent Application No. 2005/0105350 to Zimmerman ("Zimmerman"), in view of U.S. Patent No. 6,622,188 to Goodwin et al. ("Goodwin") and further in view of U.S. Patent No. 6,901,494 to Zumkehr et al. ("Zumkehr "). (Office Action dated December 5, 2006 attached hereto as Exhibit A).

VII. ARGUMENTS

I. Claim 40 are Patentable over Zimmerman in view of Goodwin and further in view of Zumkehr

A. The Subject Matter of Claims 40

Claim 40 reads as follows:

> 40. A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:
>
> issuing a read command to access a first memory location in the memory system;
>
> before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;
>
> retrieving read data from the first memory location;
>
> prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;
>
> in the memory system, bypassing the read data on the bidirectional memory bus;
>
> receiving the read data on the bidirectional memory bus from the memory system; and
>
> providing the write data to the bidirectional memory bus.

B. The Subject Matter Disclosed in the Zimmerman Reference

The Zimmerman reference is directed to a memory test mechanism for buffered-memory-module memory subsystems. The Zimmerman reference provides a testing method for evaluating individual memory modules and individual module-to-module memory channels independent of the host and host memory channel. The Zimmerman reference is cited by the

Examiner for disclosing a memory system that includes multiple hub-based memory modules with data paths that interlink the memory module hubs. Although the Zimmerman reference does disclose the memory system described above, it and no other reference cited by the Examiner discloses data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write data.

C. The Subject Matter Disclosed in the Goodwin Reference

The Goodwin reference is directed to an I^2C bus expansion apparatus that permits multiple bus devices of the same group to reside on an I^2C bus in a data processing system. The I^2C bus is a 2-wire bidirectional serial bus for communication between bus devices in a data processing system. The Goodwin reference is cited by the Examiner for disclosing a bidirectional data bus. Although the Goodwin reference discloses a bidirectional data bus, it and no other reference cited by the Examiner discloses data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write data.

D. The Subject Matter Disclosed in the Zumkehr Reference

The Zumkehr reference discloses a RAMBUS control and data bus connecting a RAMBUS memory controller 210 to a translator hub 220, and a SDRAM control and data bus connecting the translator hub 220 to SDRAM memory devices 161. *Zumkehr Specification*, Figure 2. SDRAM devices require write data to be sent with write commands. Therefore in prior systems, write commands were delayed until the write data could be sent from the RAMBUS memory controller to the SDRAM device via the translator hub. Therefore, both the write command and corresponding write data could not be sent until after the read latency of the previous read command was met. The Zumkehr reference, however, teaches the ability to issue a write command without sending the corresponding write data by storing the write command in a write buffer within the translator hub. By being able to send a write command without corresponding write data, the Zumkehr reference teaches the ability to issue a write command after a read command has been issued; however, the Zumkehr reference does not teach

the ability to issue the corresponding write data before the completion of the latency of the previous issued read command. *Zumkehr Specification*, column 4, lines 45-68 – column 5, lines 1-13.

In Figure 5A, the Zumkehr reference discloses a timing diagram of a memory system where the translator hub does not include a write buffer and Figure 5B shows a timing diagram where the translator hub does include a write buffer. In Figure 5A, a write command following a read command is delayed by a period corresponding to the read latency of the previous read command. In contrast, Figure 5B, which includes a write buffer in the translator hub, shows that a new write command 520B following a read command 501B can be issued before the read latency of the previously issued read command 501B is met. Once the new write command 520B is received in the translator hub, *a previous* write command 522B and corresponding write data 525B already stored in the translator hub are sent to the memory devices. However, the write data 527B associated with the new write command 520B remains in the memory controller and cannot be issued until *after* the read latency of the previously issued read command 501B is met. *Zumkehr Specification*, column 5, lines 39-44, column 6, lines 53-67 – column 7, lines 1-49 and Figures 5A and 5B. Therefore, the Zumkehr reference does not disclose or fairly suggest data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write.

E. Summary of the Rejection

The final rejection dated December 5, 2006 rejects claim 40 as being unpatentable under 35 U.S.C. § 103(a) over Zimmerman, in view of Goodwin, and further in view of Zumkehr.

In the Office Action, the Examiner rejected claim 40 under the same rationale as cancelled claim 1. *Office Action*, page 5, line 7 and page 7, lines 8-13, respectively. Under claim 1, the Examiner contends that Zumkehr discloses a write bypass circuit coupled to a direct data path and temporarily storing write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred

through the direct data path. In particular, the Examiner contends that the multiplexer or the write buffer in Figure 6 of the Zumkehr reference is analogous to the write bypass circuit of claim 1.

Claim 40 is patentably distinct from claim 1. Cancelled claim 1 disclosed a write bypass circuit coupled to a bidirectional data path capable of temporarily storing write data to allow read data to pass through the bidirectional data path and then recoupling the stored write data to the data path. Therefore, write data and read data could be on the bidirectional data path at the same time, moving in opposite directions and still avoid a data collision. Claim 1 did not require that the write command and corresponding write data be issued before completion of the read command. However, method claim 40 requires scheduling a write command to write data before completion of a previously issued read command.

It appears that the Examiner contends that the Zumkehr reference discloses a method of bypassing write data regardless of whether the latency of a previous read command is met. The Appellants contend that the Zumkehr reference does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued followed by a write command and corresponding write data, when the write command and corresponding write data are issued before the read latency is met.

F. The Zimmerman, Goodman, and Zumkehr References, in Combination or by Themselves, Do Not Disclose All of the Limitations of Claim 40

The Zumkehr reference was cited by the Examiner for disclosing a method of bypassing the read data on the bidirectional memory bus of claim 40. The Examiner contends that the multiplexer 650 or the write buffers 330 within the translator hub 220 have the capability of storing write data in order to prevent data collisions on a bidirectional data bus similar to the bypass circuit of the present application. The Zumkehr reference, however, does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued, and before the read latency is met, issuing a write command and corresponding write.

As described above, the Zumkehr reference discloses a bus connecting a RAMBUS memory controller 210 to a translator hub 220, and an SDRAM bus connecting the translator hub 220 to SDRAM memory devices 161. The write buffer in the translator hub is capable of receiving a write command at a different time than the corresponding write data and sending the write command and corresponding write data to the SDRAM devices. *Id.* at column 5, lines 39-44 and Figure 5B. This improves the performance of the data transfer, because the write command can be issued from the memory controller without requiring the corresponding write data to be sent from the memory controller one clock cycle later. For example, a situation in which the corresponding write data can not be sent with the write command exits when a read command has already been issued. The write data must wait for the read latency of the previously issued read command to be met before it can be transferred to the translator hub. *Id.* at column 7, lines 18-20 stating "the RAMBUS memory controller 210 defers write data transfer on a write command until the read latency of a previous read command is met". Once the translator hub receives the new write command, *a previously issued* write command and corresponding write data that were stored in the translator hub *before* the read command was issued may be sent to the memory devices before the read latency of the read command is complete. *See, Id.* at column 6, lines 53-67 – column 7, lines 1-49, and Figure 5B. Therefore, only the write data that was already issued and located on the translator hub may go onto the data bus after a subsequent read command is issued. If write data were issued from the memory hub after a read command was issued, there would be a collision on the RAMBUS data bus as the read data is heading downstream to the memory controller and the write data is heading upstream to the translator hub. Therefore, the Zumkehr reference does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued, but before the read latency is met, issuing a write command *and corresponding write data*.. Neither the Zimmerman reference nor the Goodman reference make up for the deficiencies of the Zumkehr reference.

Turning now to the claims, the Zimmerman, Goodman, and Zumkehr references, in combination or alone, do not disclose all the limitations of claim 40. A claim

rejected under 35 U.S.C. § 103(a) must teach or suggest all of the claim limitations. M.P.E.P. 706.02(j).

Method claim 40 requires, in part, issuing a read command, *before completion of the read command*, scheduling a write command, retrieving the read data, but prior to receiving the read data from the memory system, providing write data corresponding to the write command to the bidirectional memory bus, and in the memory system, bypassing the read data on the bidirectional memory bus. As alluded to above, the Zumkehr reference fails to disclose or suggest the above limitation. Rather, the Zumkehr reference waits for the read latency of a read command to end before issuing the write data that corresponds to a write command issued after the read command. In contrast, method claim 40 requires providing write data to the bidirectional memory bus prior to receiving the read data from the memory system. Therefore, claim 40 is allowable over the Zumkehr reference.

Neither the Zimmerman reference nor the Goodwin reference make up for the deficiencies in the Zumkehr reference discussed above. In fact, the Examiner explicitly admits in the Final Office Action dated December 5, 2006 that neither the Zimmerman reference nor the Goodwin reference disclose a bypath data path. *Office Action*, page 4, line 6.

For all of the reasons explained above, neither the Zumkehr reference, the Zimmerman reference, nor the Goodwin reference, in combination or by themselves, disclose or fairly suggest all elements of claim 40 in the present application. Therefore, the rejection of claim 40, as well as claims dependent thereon, should be reversed.

VIII. CLAIMS APPENDIX

The text of the claims involved in the appeal are:

40. A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

IX. EVIDENCE APPENDIX

1. Office Action dated December 5, 2006 and prior art cited therein attached hereto as Exhibit A.

2. Response dated February 5, 2007 attached hereto as Exhibit B.

3. Supplemental Response dated June 5, 2007 attached hereto as Exhibit C.

4. Applicants' Specification, filed February 5, 2004 attached hereto as Exhibit D.

X. RELATED PROCEEDINGS APPENDIX

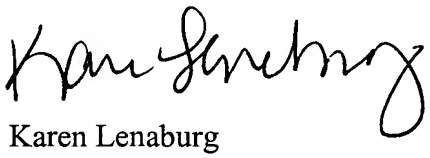
None.

XI. CONCLUSION

For all of the reasons stated above, the rejection of claims 40-43 should be reversed.

Respectfully submitted,

DORSEY & WHITNEY LLP



Karen Lenaburg
Registration No. 58,571

KL:sp

Enclosures:
Postcard
Check
Fee Transmittal (+ copy)
Appeal Brief Transmittal (+copy)

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
Tel: (206) 903-2399
Fax: (206) 903-8820

IDS REFERENCES

~~FOR~~ Exhibit A

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,583	02/05/2004	Douglas A. Larson	501296.01 (30266/US)	6732

7590 12/05/2006

Kimton N. Eng, Esq.
DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101

EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

FINAL REJECTION

2 mo. Response Due: February 5, 2007
3 mo. Response Due: March 5, 2007
Notice of Appeal Due: June 5, 2007
(6 mo. period ends/3 mo. ext. of time required - will go abandoned)

AJS

Office Action Summary	Application No.	Applicant(s)	
	10/773,583	LARSON ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,11-15,21-25 and 32-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,11-15,21-25 and 32-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 6/19/2006
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-43 have been presented for examination in this application. In response to the last office action, claims 1-3,11-13,21-23,32,36,40 have been amended, claims 5-10,16-20,26-31 have been canceled. As the result, claims 1-4,11-15,21-25,32-43 are pending in this application.

Claims 1-4,11-15,21-25,32-43 are rejected.

All rejections and objections not explicitly repeated below are withdrawn.

Applicant's amendments/remarks filed 9/19/06 have been fully considered but they are mooted in view of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

The information disclosure statements filed 9/19/06 fails to comply with the provisions of 37 CFR 1.97, 1.98 because it does not list any prior art to be considered. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,4,11,14-15,21,24-25,32-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350), in view of Goodwin et al (US 6622188), and further in view of Zumkehr (US 6901494).

As in claim 1, Zimmerman describes a memory hub for a hub-based memory module (Zimmerman's Fig 2: MMB, paragraph 17), comprising: first and second link interfaces for coupling to respective data busses; a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces (Zimmerman's Fig 2, links 112 on both sides of MMB; paragraphs 15);

Zimmerman does not disclose the claim's aspect of a bidirectional data bus operable to transfer both read and write data. However, Goodwin discloses a mechanism in which multiple memory devices are connected to a bidirectional bus as depicts in Goodwin's Fig 2: Expansion devices. It would have been obvious to one of ordinary skill in the art at the time of invention to include bi directional bus mechanism as suggested by Goodwin in Zimmerman's system thereby further allow read and write data in expansion devices such as memory devices to be transferred effectively over the same bidirectional data bus (Goodwin's column 1 lines 10-35). Zimmerman

discloses first and second link interfaces for coupling to respective portions of the bus the portion of the data bus (i.e Host side and downstream sides of the links 132, 142, each segment represent a portion of the data bus). Goodwin further discloses the expansion memory #216 having the direct data path (SCL 236 through which data is transferred between the first (i.e link to expansion memory 215) and second link (i.e link to expansion memory 218) interfaces, Zimmerman and Goodwin do not expressly disclose the claim's detail of bypath data path. However, Zumkehr's discloses a bypath data path having a write bypass circuit coupled to the direct data path and temporarily store the write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred through the direct data path (Zumkehr's Fig 7 #730 discloses the circuits in the translator hub providing a direct data path, in which the write data received by the translator hub (Fig 2: #220) is immediately and directly forwarding to the downstream device; Zumkehr's Fig 6 discloses a multiplexer (i.e write by pass circuit) that allowing temporary stored the write data while allowing the read data to be transferred through the direct data path, directly to the upstream device; subsequently the multiplexer recouple the stored write data and sending to the downstream device; Zumkehr's column 7 lines 17-23 discloses the write command received by the translator circuit must be delayed and allowing the read command to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory controller hub circuits and methods as suggested by Zumkehr in Zimmerman's system to allow transferring read data while

temporary storing write data, thereby resulting in more efficiently usage of the memory bus in the system (Zumkehr's column 6 lines 35-60; read and write data transferring through the same bidirectional data bus Fig 3: #350 data signals).

As in claim 4, Zimmerman's Fig 5 describes a memory device interface coupled to the data path, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

Claims 11,21,32,36 rejected based on the same rationale as in the rejection of claim 1.

Claims 14,24 rejected based on the same rationale as in the rejection of claim 4.

As in claim 15, Zimmerman discloses a memory controller (Fig 2: MMB) coupled to a data path through a memory controller bus (Zimmerman's Fig 2: 112); and further coupled to at least one of the plurality of memory devices through a memory device bus (MMB couples to memory device DRAM obviously vie DRAM memory device bus), a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device (Zimmerman's paragraph 15 discloses the buffered memory modules/controller logic to store the memory requests and to store the memory data receiving from the host).

Claim 21 rejected based on the same rationale as in the rejection of claim 1.Zimmerman's Fig 1 further discloses a processor (Zimmerman's Fig 1: #20) and processor bus connecting the processor to the system controller (Zimmerman's Fig 1: #30 MCH), which obviously having associating ports connecting to peripheral devices such as memory data storage devices

(Zimmerman's Fig 2: DRAM); a memory module (Zimmerman's Fig 3a) comprising memory hub (Fig 2: MMB). The remaining limitation of claim 21 is rejected based on the same rationale as of claim 1.

Claim 25 rejected based on the same rationale as of claim 15.

As in claim 33, Zumkehr's column 7 lines 17-23 discloses the write command received by the translator circuit must be delayed and allowing the read command to be issued earlier and, to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals.

As in claim 34, Zumkehr describes translator circuit to translate a write command to an sdram write command for the memory device, in addition to the FIFO queue for other write commands being received (Zumkehr's column 5 lines 5-12).

As in claim 35, Zimmerman discloses wherein the memory system includes a plurality of memory modules coupled in series on the memory bus (Zimmerman's Fig 2 DRAM memory modules #120, #130 in serial on the memory bus), and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed (Zimmrman's Fig 2 discloses writing to memory module #130 located downstream from memory module #120 in which the read data is accessed by the host #110).

Claim 37 rejected based on the same rationale of claim 33.

As in claim 38, Zumkehr's describes the write buffer to temporary store write data request (zumkerhr's Fig 3: #330).

As in claim 39, the claim recites wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus. Zumkehr further describes the write buffer in MMB is provided to temporary store data from host and thus decoupling the host to handle another accessing data on the memory bus (Zumkehr's Fig 5)

Claim 40 rejected based on the same rationale as of claim 1. Zimmerman further discloses a memory system with multiple buffered memory modules; each memory buffer module can buffer write and read command issued from the host (Fig 2: #110). Thus the host can continue issuing commands to these buffered memory modules in concurrently manner, that is the read command can be issued to memory module Fig 2: #130 before issuing the write command to memory module Fig 2: #120.

As in claim 41, the claim rejected based on the same rationale as of claim 40. Zumkehr's column 7 lines 17-23 further discloses the write command received by the translator circuit must be delayed for a time period and allowing the read command to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals. Therefore the collision on the bi-direction data bus can be averted.

As in claims 42-43, Zumkehr discloses the write data is stored temporary in Fig 3: #330 to avoid the collision with the read data receiving from bi-directional data signal Fig 2: 350's

data signals (claim 42); wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus (claim 43; Zumkehr discloses a FIFO to temporary store write commands (i.e sending the write data of the first write command to at least one memory module, receiving read command, storing the data of the second write command in the FIFO before decoupling and allowing the data of a read travels through the memory bus (from Fig 3: #350 data signals to the host, Fig 3: #310 data signal).

Claims 2-3,12-13,22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350), in view of Goodwin et al (US 6622188), Zumkehr (US 6901494) as applied to claims 1,11,21 respectively, and in view of Garcia et al (US 6782435).

As in claim 2, although Zumkehr's Fig 6: #650 discloses the multiplexer providing the directly data path (read data) and the bypass data path (write data), Zumkehr does not expressly disclose the claim's detail of the multiplexer. However, Garcia's Fig 2 teaches in detail a multiplex circuit comprises a multiplexer, a bypass selection signal, and a register to temporary store write data being received. It would have been obvious to one of ordinary skill in the art at the time of invention to include the temporary storage and the multiplexer circuits as suggested by Garcia in Zimmerman's system to temporary reordering the transmitting data thereby allowing accessing memory device with minimum latency and maximizing the throughput of he overall system (Garcia's column 1, lines 48-62).

As in claims 3, the claim recite wherein the write bypass circuit further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register. The claim rejected based on the same rationale as in the rejection of claim 2.

Claims 12,22 rejected based on the same rationale as of claim 2.

Claims 13,23 rejected based on the same rationale as of claim 3.

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

Regarding remarks on pages 11-12 for the Zimmerman's expressly teaching of the bidirectional data bus. It's mooted in view of the new reference Goodwin et al, new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

Regarding the remark on pages 12-17, Applicant contends that Zumkehr does not provide a direct data path for the write data to be provided to the down stream device (i.e the sdram device). Examiner respectfully disagrees. Zumkehr's Fig 6 discloses a multiplexer in the translator hub that provides a data path directly to the downstream device, when it received the write data sent from the host's Fig 3: #210; receiving at its buffer Zumker's Fig 3: #330 and sending directly to down stream devices Fig 3: #161. Examiner notes that the same mechanism is

disclosed in specification's Fig 3, that is host's data is received at a receiving buffer Fig 3: 302 and subsequently it is sent directly to down stream device.

Applicant contends that Zumkehr's buffering circuits do not provide avoiding the data collision between data heading the opposite directions on the bidirectional data paths. Examiner respectfully disagrees, Zumkehr discloses write buffers that temporary store write data of write requests so that the read data of the read command can be sent on the opposite direction toward the host on the same bidirectional bus, Fig 3: #350 data signals. Thus the write data toward the down stream device is temporary stored, delay and avoids the collision with the read data traveling in opposite direction on the same bidirectional data bus (see Zumkehr's column 6 lines 22-30).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
11/29/06

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 501296.01 (30266/US)	APPLICATION NO. 10/773,583
INFORMATION DISCLOSURE STATEMENT *(Use additional sheets if necessary)*		APPLICANT(S) Douglas A. Larson and Jeffrey J. Cronin	
		FILING DATE February 5, 2004	GROUP ART UNIT 2188

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
DD	AA	6,324,485 B1	11/27/01	Ellis	702	117	
	AB	6,526,483 B1	02/25/03	Cho et al.	711	154	
	AC	6,636,912 B2	10/21/03	Ajanovic et al.	710	105	
	AD	2003/0005344 A1	01/02/03	Bhamidipati et al.	713	400	
	AE	2003/0156581 A1	08/21/03	Osborne	370	389	
	AF	2003/0229762 A1	12/11/03	Maiyuran et al.	711	137	
	AG	2005/0015426 A1	01/20/05	Woodruff et al.	709	200	
	AH	2005/0149603 A1	07/07/05	DeSota et al.	709	200	
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AM							
	AN							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

DD	AO	Rambus, Inc., "Direct Rambus™ Technology Disclosure", October 1997. pp. 1-16.
	AP	
	AQ	

EXAMINER	DATE CONSIDERED
Sue Doan	11/28/06

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

Notice of References Cited	Application/Control No. 10/773,583	Applicant(s)/Patent Under Reexamination LARSON ET AL.	
	Examiner Duc T. Doan	Art Unit 2188	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,622,188	09-2003	Goodwin et al.	710/105
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

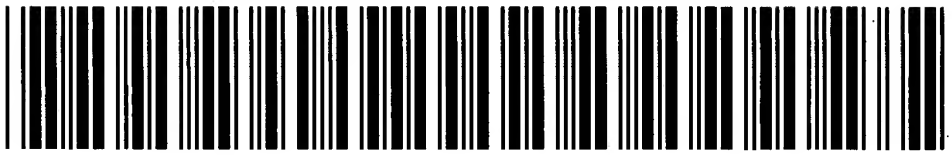
*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

IDS REFERENCES



☐ ~~FOR~~ Exhibit B

RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE - EXAMINING GROUP 2100

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

February 7, 2007 _____
Date Sherri A. Phillips

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/773,583	Confirmation No.	: 6732
Applicants	: Douglas A. Larson and Jeffrey J. Cronin		
Filed	: February 5, 2004	Attorney Docket No.:	501296.01 (30266/US)
Art Unit	: 2188	Customer No.	: 27,076
Examiner	: Duc T. Doan		
Title	: APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 C.F.R. § 1.116

Sir:

Applicants acknowledge receipt of the Office Action dated December 5, 2006. Please amend the above-captioned patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks begin on page 7 of this paper.

Amendments to the Specification:

Please replace paragraph [23] with the following amended paragraph:

--In operation, WR_DATA_IN received by the data bypass circuit 300 is driven through the input buffer 302 and is provided to the first input of the multiplexer 306. The WR_DATA_IN is also saved in the bypass register/FIFO 304. In response to an inactive ACT signal, an active EN signal is generated by the bypass select logic 308. The active EN signal enables output by the input/output buffer 310 and couples the output of the input buffer 302 to the input of the input/output buffer 310 through the multiplexer 306. As a result, the WR_DATA_IN is provided directly to the input of the input/output buffer 310 and the WR_DATA_IN is provided through the data bypass circuit 300 without any bypass. However, in response to an active ACT signal, the bypass select logic 308 generates an inactive EN signal, disabling the output function of the input/output buffer 310 and placing its output in a high-impedance state. Additionally, the inactive EN signal couples the input of the input/output buffer 310 to the output of the bypass register/FIFO 304. In this manner, the WR_DATA_IN is received by the data bypass circuit 300, stored by the bypass register/FIFO ~~306~~ 304, and applied to the input of the input/output buffer 310. However, due to the inactive state of the EN signal, the WR_DATA_IN is not provided as output data WR_DATA_OUT by the input/output buffer 310. As a result, the WR_DATA_IN is held in a bypass state until the ACT signal becomes inactive, at which time, the EN signal become active again, enabling the input/output buffer 310 to provide the WR_DATA_IN as WR_DATA_OUT data. The multiplexer 306 is also switched back to coupling the output of the input buffer 302 directly to the input of the input/output buffer 310 to allow WR_DATA_IN to pass through the data bypass circuit unhindered.--

Please replace paragraph [25] with the following amended paragraph:

--In Figure 4, it is assumed that the memory hub controller 128 has just issued read and write commands, with the read command sequenced prior to the write command. The read command is directed to the memory module 130b and the write command is directed to the memory module 130c. That is, the memory module to which data will be written is further downstream than the memory module from which data is read. In response to the read command, the memory hub 140b begins retrieving the read data (RD) from the memory device 148b, as indicated in Figure 4 by the "(1)". With the read command issued, the write command

is then initiated, and the write data (WD) is provided onto the high-speed link 134. However, since the memory hub controller 128 is expecting the RD to be returned from the memory module 130b, the memory hub 140a is directed to capture the WD in its data bypass circuit 286a. As a result, the ~~memory hub~~ data bypass circuit 286a captures the WD to clear the high-speed link 134, as indicated in Figure 4 by the "(2)", for the RD to be returned to the memory hub controller 128. When the memory hub 140b has retrieved the RD from the memory device 148b, and has indication from the memory hub 140a that the WD has been successfully captured by the data bypass circuit 286a, the RD is then provided to the memory hub controller 128 through the high-speed link 134, as indicated in Figure 4 by the "(3)" to complete the read request. Upon the RD passing through the memory hub 140a on its way to the memory hub controller 128, the memory hub 140a releases the WD from the data bypass circuit 286a to continue its way to the memory hub 140c. The WD is provided to the memory hub 140c through the high-speed link, which is now clear between the memory hub 140a and 140c. Upon reaching the memory hub 140c, the WD is written in the memory device 148c, as shown in Figure 4 by the "(4)".--

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 1-4, 11-15 and 21-25, and amend claims 32 and 40 as follows:

Listing of Claims:

1-31. (Canceled)

32. (Currently Amended) A method for writing data to a memory location in a memory system coupled to a bidirectional memory bus transmitting both read and write data, comprising:

~~accessing read data in~~ issuing a read command to the memory system;

providing a write command and corresponding write data to the memory system on the bidirectional memory bus, after issuing the read command;

coupling the write data to a register in the memory system for temporary storage of the write data to allow the read data to be returned on the bidirectional data bus after the write data is provided to the same and before the write data has been written;

coupling the read data to the bidirectional memory bus and providing the read data for reading;

coupling the write data stored in the register to the bidirectional memory bus; and

writing the write data to the memory location.

33. (Original) The method of claim 32, further comprising issuing a read command to the memory system prior to issuing a write command to the memory system.

34. (Original) The method of claim 32 wherein providing the write data to the memory system comprises providing the write data through at least one memory module of the memory system prior to coupling the write data to the register.

35. (Original) The method of claim 32 wherein the memory system includes a plurality of memory modules coupled in series on the memory bus, and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed.

36. (Previously Presented) A method for executing memory commands in a memory system having a memory bus on which both read and write data can be coupled, the method comprising:

issuing a read command to the memory system;

issuing a write command to a memory location in the memory system and providing write data for the write command to the memory bus of the memory system after issuing the read command;

accessing read data in the memory system;

in the memory system, decoupling the write data from the memory bus;

receiving the read data on the memory bus from the memory system;

recoupling the write data to the memory bus; and

resuming the write command to the memory location.

37. (Original) The method of claim 36 wherein issuing the read command to the memory system precedes issuing the write command to the memory system.

38. (Original) The method of claim 36, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

39. (Original) The method of claim 36 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

40. (Currently Amended) A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. (Original) The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. (Original) The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. (Original) The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

REMARKS

The specification has been amended in order to resolve obvious errors. No new matter was added.

The Applicants would like to thank the Examiner for the telephone interview conducted on February 1, 2007. During the interview the Applicants stated that the write buffer in the Zumkehr patent, Patent No. 6,901,494, does not disclose a bypass data path having a write bypass circuit coupled to a direct data pass operable to temporarily store the write data to allow read data to be transferred through the direct data path. The Examiner did not agree. The Examiner suggested that the Applicants draft an argument for his Supervisor to review. The Applicants would like to thank the Examiner and his Supervisor for the opportunity to have the argument reviewed by the Examiner's Supervisor.

After the interview, Applicants' attorney spent a great deal of time studying the Zumkehr patent and now has a better understanding of the Examiner's position. Applicants admit that there are some similarities between subject matter disclosed in the present application and the Zumkehr patent for situations in which the write data is passed from the controller 210 to the translator hub 220 *before* a read command is applied to the hub 220. For example in Zumkehr, write data is passed from the controller 210 to the translator hub 220 before a read command is passed from the controller 210 to the translator hub 220 and from the translator hub 220 to the appropriate memory device 161. The read data is then passed from the memory device 161 to the translator hub 220. A write command corresponding to the previous write data is then sent from the controller 210 to the translator hub 220. During the time the read data is being sent from the translator hub 220 to the controller 210, the write data also is sent from the translator hub 220 to the appropriate memory device 161. Therefore, data is being transferred on the bus at the same time. *Zumkehr Specification*, Figure 5B and column 6, lines 53-67 - column 7, lines 1-49.

On the other hand, there are differences that are significant for situations where, as in applicants' system, the write command and corresponding write data are output from a controller *after* the read command are output from the controller. In the Zumkehr system, when a read command is issued to the memory system before a write command and corresponding write data are issued to the memory system, the controller 210 defers the transfer of the write data from the controller 210 to the translator hub 220 until the read latency is met. *Zumkehr*

specification, column 7, lines 15-20 and Figure 5B. The disclosed system, however, does not require that the read latency be met before transferring the write command and corresponding write data from the controller to the memory system. Rather, the write command and corresponding write data may be provided to the memory system after the read command is issued to the memory system. This means that read data will be going in one direction to the controller and write data will be going in the opposite direction to a memory device at the same time. In order to prevent a collision on the data bus, the write data is decoupled from the bidirectional data bus by the bypass register. Once the read data has passed the bypass register, the write data is recoupled to the bidirectional data bus. Because the Zumkehr patent requires the write data to be already stored in the hub before a read command is issued, it does not meet all of the requirements for the method claims in the present application.

The Applicants propose canceling the apparatus claims, 1-4, 11-15, and 21-25 in the present application. The Applicants further propose filing a continuation application to prosecute amended apparatus claims separately from the method claims of the current application. In addition, the Applicants propose amending independent method claim 32 in the present application so that it has limitations similar to those already included in independent method claims 36 and 40, that the read command is issued to the memory system before the write data is provided to the memory system.

Upon the Examiner's acceptance of the proposed changes, all of the claims remaining in the application are clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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IDS REFERENCES

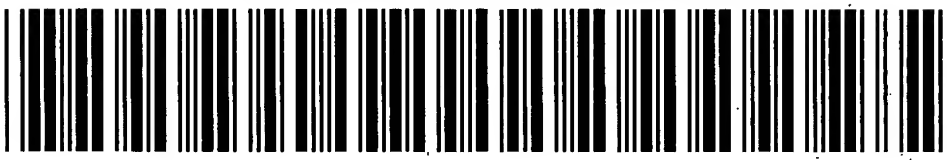
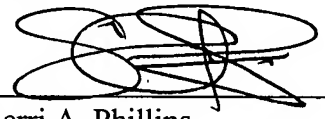


Exhibit C

RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE - EXAMINING GROUP 2100

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

June 5, 2007 

Date Sherri A. Phillips

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/773,583	Confirmation No.	: 6732
Applicants	: Douglas A. Larson and Jeffrey J. Cronin		
Filed	: February 5, 2004	Attorney Docket No.:	501296.01 (30266/US)
Art Unit	: 2188	Customer No.	: 27,076
Examiner	: Duc T. Doan		
Title	: APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL RESPONSE UNDER 37 C.F.R. § 1.116

Sir:

Applicants acknowledge receipt of the Office Action dated December 5, 2006. Further to the response filed February 7, 2007, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 4 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 32-39.

Listing of Claims:

1-39. (Canceled)

40. (Previously Presented) A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. (Original) The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. (Original) The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. (Original) The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

REMARKS

Applicants filed a Notice of Appeal on April 5, 2007. Applicants acknowledge receipt of the Office Action dated December 5, 2006, and further to the response filed February 7, 2007, request the cancellation of claims 32-39.

Respectfully submitted,

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IDS REFERENCES

~~FOR~~ Exhibit D

APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM

TECHNICAL FIELD

The present invention relates to memory systems, and more particularly, to memory modules having a data bypass for preventing data collision on a bi-direction data bus.

BACKGROUND OF THE INVENTION

Computer systems use memory devices, such as dynamic random access memory ("DRAM") devices, to store data that are accessed by a processor. These memory devices are normally used as system memory in a computer system. In a typical computer system, the processor communicates with the system memory through a processor bus and a memory controller. The memory devices of the system memory, typically arranged in memory modules having multiple memory devices, are coupled through a memory bus to the memory controller. The processor issues a memory request, which includes a memory command, such as a read command, and an address designating the location from which data or instructions are to be read. The memory controller uses the command and address to generate appropriate command signals as well as row and column addresses, which are applied to the system memory through the memory bus. In response to the commands and addresses, data are transferred between the system memory and the processor. The memory controller is often part of a system controller, which also includes bus bridge circuitry for coupling the processor bus to an expansion bus, such as a PCI bus.

In memory systems, high data bandwidth is desirable. Generally, bandwidth limitations are not related to the memory controllers since the memory controllers sequence data to and from the system memory as fast as the memory devices allow. One approach that has been taken to increase bandwidth is to increase the speed of the memory data bus coupling the memory controller to the memory devices. Thus, the same amount of

information can be moved over the memory data bus in less time. However, despite increasing memory data bus speeds, a corresponding increase in bandwidth does not result. One reason for the non-linear relationship between data bus speed and bandwidth is the hardware limitations within the memory devices themselves. That is, the memory controller has to schedule all memory commands to the memory devices such that the hardware limitations are honored. Although these hardware limitations can be reduced to some degree through the design of the memory device, a compromise must be made because reducing the hardware limitations typically adds cost, power, and/or size to the memory devices, all of which are undesirable alternatives. Thus, given these constraints, although it is easy for memory devices to move "well-behaved" traffic at ever increasing rates, for example, sequel traffic to the same page of a memory device, it is much more difficult for the memory devices to resolve "badly-behaved traffic," such as bouncing between different pages or banks of the memory device. As a result, the increase in memory data bus bandwidth does not yield a corresponding increase in information bandwidth.

In addition to the limited bandwidth between processors and memory devices, the performance of computer systems is also limited by latency problems that increase the time required to read data from system memory devices. More specifically, when a memory device read command is coupled to a system memory device, such as a synchronous DRAM ("SDRAM") device, the read data are output from the SDRAM device only after a delay of several clock periods. Therefore, although SDRAM devices can synchronously output burst data at a high data rate, the delay in initially providing the data can significantly slow the operating speed of a computer system using such SDRAM devices. Increasing the memory data bus speed can be used to help alleviate the latency issue. However, as with bandwidth, the increase in memory data bus speeds do not yield a linear reduction of latency, for essentially the same reasons previously discussed.

Although increasing memory data bus speed has, to some degree, been successful in increasing bandwidth and reducing latency, other issues are raised by this

approach. For example, as the speed of the memory data bus increases, loading on the memory bus needs to be decreased in order to maintain signal integrity since traditionally, there has only been wire between the memory controller and the memory slots into which the memory modules are plugged. Several approaches have been taken to accommodate the increase in memory data bus speed. For example, reducing the number of memory slots, adding buffer circuits on a memory module in order to provide sufficient fanout of control signals to the memory devices on the memory module, and providing multiple memory device interfaces on the memory module since there are too few memory module connectors on a single memory device interface. The effectiveness of these conventional approaches are, however, limited. A reason why these techniques were used in the past is that it was cost-effective to do so. However, when only one memory module can be plugged in per interface, it becomes too costly to add a separate memory interface for each required memory slot. In other words, it pushes the system controllers package out of the commodity range and into the boutique range, thereby, greatly adding cost.

One recent approach that allows for increased memory data bus speed in a cost effective manner is the use of multiple memory devices coupled to the processor through a memory hub. In a memory hub architecture, or a hub-based memory sub-system, a system controller or memory controller is coupled over a high speed bi-directional or unidirectional memory controller/hub interface to several memory modules. Typically, the memory modules are coupled in a point-to-point or daisy chain architecture such that the memory modules are connected one to another in series. Thus, the memory controller is coupled to a first memory module, with the first memory module connected to a second memory module, and the second memory module coupled to a third memory module, and so on in a daisy chain fashion.

Each memory module includes a memory hub that is coupled to the memory controller/hub interface and a number of memory devices on the module, with the memory hubs efficiently routing memory requests and responses between the controller and the memory devices over the memory controller/hub interface. Computer systems employing

this architecture can use a high-speed memory data bus since signal integrity can be maintained on the memory data bus. Moreover, this architecture also provides for easy expansion of the system memory without concern for degradation in signal quality as more memory modules are added, such as occurs in conventional memory bus architectures.

Although computer systems using memory hubs may provide superior performance, they may often fail to operate at optimum efficiency for a variety of reasons. One such reason is the issue of managing data collision between data flowing to and from the memory controller through the memory hubs. In conventional memory controllers, one approach taken to avoid data collision is to delay the execution of one memory command until the completion of another memory command. For example, with a conventional memory controller, a write command issued after a read command is not allowed to begin until the read command is nearly completed in order to avoid the read (i.e., inbound) data colliding with the write (i.e., outbound) data on the memory bus. However, forcing the write command to wait effectively reduces bandwidth, which is inconsistent with what is typically desired in a memory system.

SUMMARY OF THE INVENTION

One aspect of the present invention is directed to a memory hub having a data bypass circuit. The memory hub includes first and second link interfaces for coupling to respective data busses, a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces. The memory hub further includes a write bypass circuit coupled to the data path for coupling write data on the data path and temporarily storing the write data to allow read data to be transferred through the data path while the write data is temporarily stored. In another aspect of the invention, a method for writing data to a memory location in a memory system coupled to a memory bus is provided. The method includes accessing read data in the memory system, providing write data to the memory system on the memory bus, and coupling the write data to a register for temporary storage of the write data. While the data is temporarily stored,

the read data is coupled from the memory bus and provided for reading. The write data is recoupled to the memory bus and written to the memory location.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a computer system having memory modules in a memory hub architecture in which embodiments of the present invention can be implemented.

Figure 2 is a partial block diagram of a memory hub according to an embodiment of the present invention for use with the memory modules of Figure 1.

Figure 3 is a block diagram of a data bypass circuit for the memory hub of Figure 2 according to an embodiment of the present invention.

Figure 4 is a block diagram illustrating the operation of the data bypass circuit of Figure 3 for a computer system having the memory hub architecture of Figure 1 and the memory hub of Figure 2.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention are directed to a memory hub having bypass circuitry that provides data bypass for a bi-directional data bus in a hub-based memory sub-system. Certain details are set forth below to provide a sufficient understanding of various embodiments of the invention. However, it will be clear to one skilled in the art that the invention may be practiced without these particular details. In other instances, well-known circuits, control signals, and timing protocols have not been shown in detail in order to avoid unnecessarily obscuring the invention.

Figure 1 illustrates a computer system 100 according to one embodiment of the present invention. The computer system 100 includes a processor 104 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. The processor 104 includes a processor bus 106 that normally includes an address bus, a control bus, and a data bus. The processor bus 106 is typically

coupled to cache memory 108. Typically, the cache memory 108 is provided by a static random access memory ("SRAM"). The processor bus 106 is also coupled to a system controller 110, which is sometimes referred to as a bus bridge.

The system controller 110 serves as a communications path to the processor 104 for a variety of other components. For example, as shown in Figure 1, the system controller 110 includes a graphics port that is typically coupled to a graphics controller 112. The graphics controller is typically coupled to a video terminal 114, such as a video display. The system controller 110 is also coupled to one or more input devices 118, such as a keyboard or a mouse, to allow an operator to interface with the computer system 100. Typically, the computer system 100 also includes one or more output devices 120, such as a printer, coupled to the processor 104 through the system controller 110. One or more data storage devices 124 are also typically coupled to the processor 104 through the system controller 110 to allow the processor 104 to store data or retrieve data from internal or external storage media (not shown). Examples of typical storage devices 124 include hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs).

The system controller 110 includes a memory hub controller 128 that is coupled to memory hubs 140 of several memory modules 130a, 130b, 130c, . . . 130n. The memory modules 130 serve as system memory for the computer system 100, and are preferably coupled to the memory hub controller 128 through a high-speed bi-directional memory controller/hub interface 134. The memory modules 130 are shown coupled to the memory hub controller 128 in a point-to-point arrangement in which the memory controller/hub interface 134 is coupled through the memory hubs 140 of the memory modules 130. That is, the memory controller/hub interface 134 is a bi-directional bus that couples the memory hubs 140 in series. Thus, information on the memory controller/hub interface 134 must travel through the memory hubs 140 of "upstream" memory modules 130 to reach a "downstream" destination. For example, with specific reference to Figure 1, information transmitted from the memory hub controller 128 to the memory hub 140 of the

memory module 130c will pass through the memory hubs 140 of the memory modules 130a and 130b.

It will be appreciated, however, that topologies other than the point-to-point arrangement of Figure 1 may also be used. For example, a coupling arrangement may be used in which a separate high-speed link (not shown) is used to couple each of the memory modules 130 to the memory hub controller 128. A switching topology may also be used in which the memory hub controller 128 is selectively coupled to each of the memory modules 130 through a switch (not shown). Other topologies that may be used will be apparent to one skilled in the art. Additionally, the memory controller/hub interface 134 coupling the memory modules to the memory hub controller may be an electrical or optical communication path. However, other types of communications paths can be used for the memory controller/hub interface 134 as well. In the event the memory controller/hub interface 134 is implemented as an optical communication path, the optical communication path may be in the form of one or more optical fibers. In such case, the memory hub controller 128 and the memory modules will include an optical input/output port or separate input and output ports coupled to the optical communication path, as well known in the art.

The memory hubs 140 control access to memory devices 148 of the respective memory module 130. In Figure 1, the memory devices are illustrated as synchronous dynamic random access memory ("SDRAM") devices. However, memory devices other than SDRAM devices may also be used. As also shown in Figure 1, the memory hub is coupled to four sets of memory devices 148 through a respective memory bus 150. Each of the sets includes four memory devices 148 for a total of 20 memory devices 148 for each memory module 130. The memory busses 150 normally include a control bus, an address bus, and a data bus, as known in the art. However, it will be appreciated by those ordinarily skilled in the art that other bus systems, such as a bus system using a shared command/address bus, may also be used without departing from the scope of the present invention. It will be further appreciated that the arrangement of the

memory devices 148, and the number of memory devices 148 can be modified without departing from the scope of the present invention.

Figure 2 illustrates a portion of the memory hub 140 according to an embodiment of the present invention. The memory hub 140 includes a local hub circuit 214 coupled to the memory controller/hub interface 134 (Figure 1). The local hub circuit 214 is further coupled to memory devices 148 through the memory bus 150. The local hub circuit 214 includes control logic for processing memory commands issued from the memory controller 128 and for accessing the memory devices 148 over the memory bus 150 to provide the corresponding data when the memory command is directed to the respective memory module 130. The design and operation of such control logic is well known by those ordinarily skilled in the art, and consequently, a more detailed description has been omitted from herein in the interest of brevity. The memory hub 140 further includes a data bypass circuit 286 coupled to the local hub circuit 214. As will be explained in more detail below, the data bypass circuit 286 is used to temporarily capture data passing to a distant memory hub, which allows data returning from another distant memory hub to pass through the memory hub 140 before the captured data continues onto the distant memory hub. Thus, the data bypass circuit 286 provides a data bypass mechanism that can be used to avoid data collisions on the bi-directional memory controller/hub interface 134 to which the memory hub 140 is coupled.

As previously discussed, one approach taken by conventional memory sub-systems to avoid data collision is to delay the execution of one memory command until the completion of another memory command. For example, in typical memory systems a write command issued after a read command would not have been allowed to start until near the completion of the read command in order to avoid the read (i.e., inbound) data colliding with the write (i.e., outbound) data on the memory controller/hub interface 134. In contrast, by employing the memory hub 140 having the data bypass circuit 286, write commands issued after a read command can be sequenced earlier than compared with

conventional memory systems, and consequently, memory commands scheduled after the earlier scheduled write command can be executed sooner as well. .

Figure 3 illustrates a data bypass circuit 300 according to an embodiment of the present invention. The data bypass circuit 300 can be substituted for the data bypass circuit 286 (Figure 2) and can be implemented using conventional designs and circuits well known to those ordinarily skilled in the art. The data bypass circuit 300 includes an input buffer 302 that receives input write data WR-DATA_IN and provides the same to a bypass register/FIFO 304 and a first input of a multiplexer 306. An output of the bypass register/FIFO 304 is coupled to a second input of the multiplexer 306. Selection of which of the two inputs to couple to the output of the multiplexer 306 is made by an enable signal EN generated by a bypass select logic 308. The EN signal is also provided to an input/output buffer 310 as an output enable signal activating or deactivating the input/output buffer 310. The bypass select logic 308 generates the appropriate EN signal in response to an activation signal BYPASS_EN provided by the memory hub controller 128 (Figure 1). Alternatively, the BYPASS_EN signal may be provided from other memory hubs (not shown) that are part of the same memory system. The circuitry of the data bypass circuit is conventional, and it will be appreciated that the circuits of the data bypass circuit 300 can be implemented using conventional designs and circuitry well known in the art.

In operation, WR_DATA_IN received by the data bypass circuit 300 is driven through the input buffer 302 and is provided to the first input of the multiplexer 306. The WR_DATA_IN is also saved in the bypass register/FIFO 304. In response to an inactive BYPASS_EN signal, an active EN signal is generated by the bypass select logic 308. The active EN signal enables output by the input/output buffer 310 and couples the output of the input buffer 302 to the input of the input/output buffer 310 through the multiplexer 306. As a result, the WR_DATA_IN is provided directly to the input of the input/output buffer 310 and the WR_DATA_IN is provided through the data bypass circuit 300 without any bypass. However, in response to an active BYPASS_EN signal, the bypass select logic 308 generates an inactive EN signal, disabling the output function of the

input/output buffer 310 and placing its output in a high-impedance state. Additionally, the inactive EN signal couples the input of the input/output buffer 310 to the output of the bypass register/FIFO 304. In this manner, the WR_DATA_IN is received by the data bypass circuit 300, stored by the bypass register/FIFO 306, and applied to the input of the input/output buffer 310. However, due to the inactive state of the EN signal, the WR_DATA_IN is not provided as output data WR_DATA_OUT by the input/output buffer 310. As a result, the WR_DATA_IN is held in a bypass state until the BYPASS_EN signal becomes inactive, at which time, the EN signal become active again, enabling the input/output buffer 310 to provide the WR_DATA_IN as WR_DATA_OUT data. The multiplexer 306 is also switched back to coupling the output of the input buffer 302 directly to the input of the input/output buffer 310 to allow WR_DATA_IN to pass through the data bypass circuit unhindered.

Operation of the data bypass circuit 286 will be described with reference to Figure 4. Figure 4 is similar to Figure 1, except that Figure 4 has been simplified. In particular, many of the functional blocks of Figure 1 have been omitted, with only the memory modules 130a-130c being shown, and represented by memory hubs 140a-140c. Only one memory device 148a-148c is shown to be coupled to a respective memory hub 140a-140c through a respective memory bus 150a-150c. As with Figure 1, the memory hubs 140a-140c are coupled by a high-speed bi-directional memory controller/hub interface 134 to a memory hub controller 128.

In Figure 4, it is assumed that the memory hub controller 128 has just issued read and write commands, with the read command sequenced prior to the write command. The read command is directed to the memory module 130b and the write command is directed to the memory module 130c. That is, the memory module to which data will be written is further downstream than the memory module from which data is read. In response to the read command, the memory hub 140b begins retrieving the read data (RD) from the memory device 148b, as indicated in Figure 4 by the "(1)". With the read command issued, the write command is then initiated, and the write data (WD) is provided

onto the memory controller/hub interface 134. However, since the memory hub controller 128 is expecting the RD to be returned from the memory module 130b, the memory hub 140a is directed to capture the WD in its data bypass circuit 286a. As a result, the memory hub 286a captures the WD to clear the memory controller/hub interface 134, as indicated in Figure 4 by the "(2)", for the RD to be returned to the memory hub controller 128. When the memory hub 140b has retrieved the RD from the memory device 148b, the RD is then provided to the memory hub controller 128 through the memory controller/hub interface 134, as indicated in Figure 4 by the "(3)" to complete the read request. Upon the RD passing through the memory hub 140a on its way to the memory hub controller 128, the memory hub 140a releases the WD from the data bypass circuit 286a to continue its way to the memory hub 140c. The WD is provided to the memory hub 140c through the high-speed link, which is now clear between the memory hub 140a and 140c. Upon reaching the memory hub 140c, the WD is written in the memory device 148c, as shown in Figure 4 by the "(4)". In an embodiment of the present invention, coordination of the data flow of the RD and WD on the memory controller/hub interface 134 and through the data bypass circuits 286 is under the control of the memory hub controller 128. For example, in the previous example the memory hub controller ensures that any WD flowing in the opposite direction of the RD is out of the way when retrieving RD from the memory module 130b. It will be appreciated, however, that in alternative embodiments data flow through the memory controller/hub interface 134 and the data bypass circuits 286 can be managed differently, such as the memory hub controller 128 sharing coordination of the data flow with the memory hubs 140.

In the previous example, the RD is returned to the memory hub controller 128 as in a conventional memory system. That is, the RD transmitted by the memory devices 148 is provided to the memory controller without any significant delay. However, by employing the previously described data bypass mechanism, write commands can be scheduled earlier than with conventional memory systems. A write command issued after a read command would not have been allowed to start until near the completion of the read

command in typical memory systems. In contrast, embodiments of the present invention allow a subsequently issued write command to be scheduled earlier, thus, reducing the time gap between read and write commands. As a result, commands scheduled behind an earlier scheduled write command have an overall reduced latency.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

1. A memory hub for a hub-based memory module, comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

2. The memory hub of claim 1 wherein the write bypass circuit comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

3. The memory hub of claim 2 wherein the write bypass circuit further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

4. The memory hub of claim 1, further comprising a memory device interface coupled to the data path, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

5. A memory hub for a hub-based memory module, comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

6. The memory hub of claim 5 wherein the data bypass circuit comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

7. The memory hub of claim 6 wherein the data bypass circuit further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

8. The memory hub of claim 5, further comprising a memory device interface coupled to the switching circuit, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

9. The memory hub of claim 8 wherein the memory device interface comprises:

a memory controller coupled to the data path through a memory controller bus and further having a memory device terminal to which a memory device can be coupled;

a write buffer coupled to the memory controller for storing memory requests; and

a cache coupled to the memory controller for storing data.

10. The memory hub of claim 5 wherein the first set of data represents write data and the second set of data represents read data.

11. A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, the memory hub comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

12. The memory module of claim 11 wherein the write bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

13. The memory module of claim 12 wherein the write bypass circuit of the memory hub further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

14. The memory module of claim 11 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

15. The memory module of claim 14 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

16. A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to at least one of the plurality of memory devices, the memory hub comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

17. The memory module of claim 16 wherein the data bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer

input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

18. The memory module of claim 17 wherein the data bypass circuit of the memory hub further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

19. The memory module of claim 16 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

20. The memory module of claim 16 wherein the first set of data represents write data and the second set of data represents read data.

21. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, the memory hub comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

22. The processor-based system of claim 21 wherein the write bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

23. The processor-based system of claim 22 wherein the write bypass circuit of the memory hub further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

24. The processor-based system of claim 21 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

25. The processor-based system of claim 24 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

26. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to at least one of the plurality of memory devices, the memory hub comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

27. The processor-based system of claim 26 wherein the data bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

28. The processor-based system of claim 27 wherein the data bypass circuit of the memory hub further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

29. The processor-based system of claim 26 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

30. The processor-based system of claim 29 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

31. The processor-based system of claim 26 wherein the first set of data represents write data and the second set of data represents read data.

32. A method for writing data to a memory location in a memory system coupled to a memory bus, comprising:

accessing read data in the memory system;

providing write data to the memory system on the memory bus;

coupling the write data to a register in the memory system for temporary storage of the write data;

coupling the read data to the memory bus and providing the read data for reading;

coupling the write data stored in the register to the memory bus; and

writing the write data to the memory location.

33. The method of claim 32, further comprising issuing a read command to the memory system prior to issuing a write command to the memory system.

34. The method of claim 32 wherein providing the write data to the memory system comprises providing the write data through at least one memory module of the memory system prior to coupling the write data to the register.

35. The method of claim 32 wherein the memory system includes a plurality of memory modules coupled in series on the memory bus, and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed.

36. A method for executing memory commands in a memory system having a memory bus, the method comprising:

issuing a read command to the memory system;

issuing a write command to a memory location in the memory system and providing write data to the memory bus of the memory system;

accessing read data in the memory system;

in the memory system, decoupling the write data from the memory bus;

receiving the read data on the memory bus from the memory system;

recoupling the write data to the memory bus; and

resuming the write command to the memory location.

37. The method of claim 36 wherein issuing the read command to the memory system precedes issuing the write command to the memory system.

38. The method of claim 36, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

39. The method of claim 36 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

40. A method for executing read and write commands in a memory system having a memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system

retrieving read data from the first memory location;

providing write data to the memory bus of the memory system;

in the memory system, bypassing the read data on the memory bus;

receiving the read data on the memory bus from the memory system; and

providing the write data to the memory bus.

41. The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

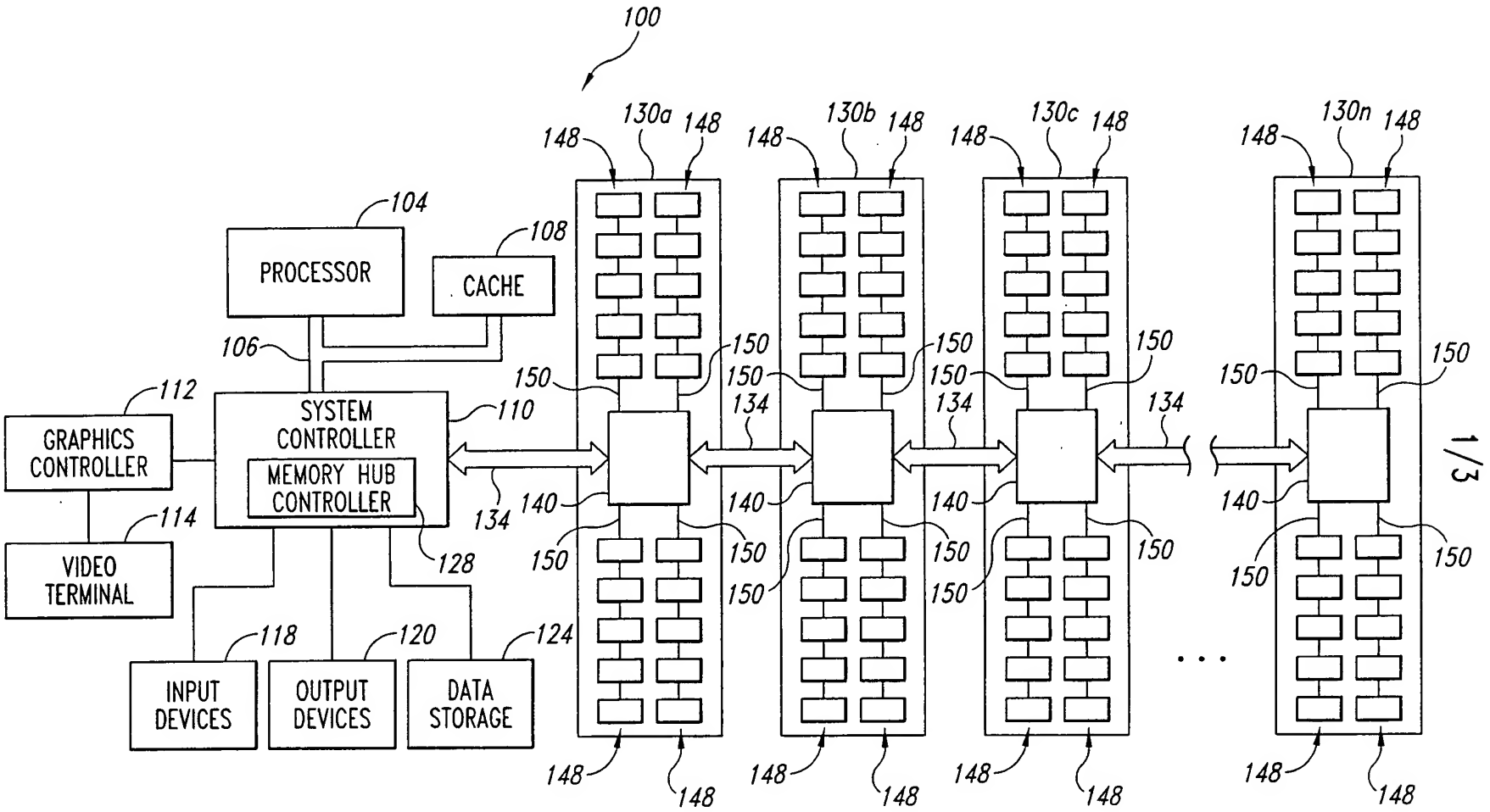
42. The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM

ABSTRACT OF THE DISCLOSURE

A memory hub includes first and second link interfaces for coupling to respective data busses, a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces, and further includes a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored. A method for writing data to a memory location in a memory system is provided which includes accessing read data in the memory system, providing write data to the memory system, and coupling the write data to a register for temporary storage. The write data is recoupled to the memory bus and written to the memory location following provision of the read data.


100
PROCESSOR
104
CACHE
108
106
SYSTEM CONTROLLER
MEMORY HUB CONTROLLER
110
GRAPHICS CONTROLLER
112
VIDEO TERMINAL
114
128
INPUT DEVICES
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OUTPUT DEVICES
120
DATA STORAGE
124
130a
130b
130c
130n
148
150
134
140

Fig. 1

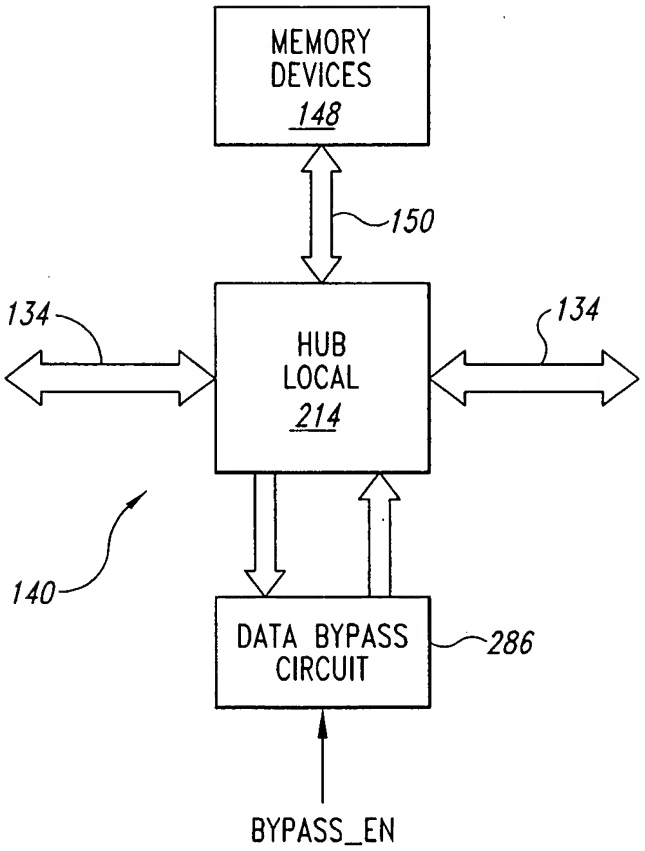

MEMORY DEVICES
148
150
134
134
HUB LOCAL
214
140
DATA BYPASS CIRCUIT
286
BYPASS_EN

Fig. 2

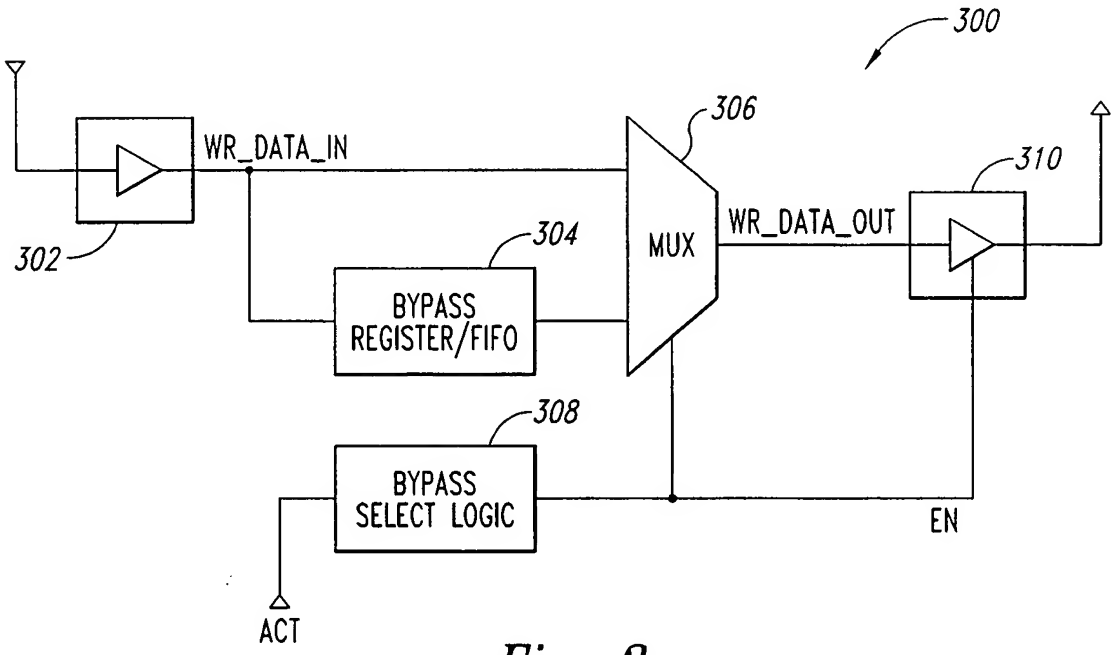

300
306
WR_DATA_IN
310
302
304
MUX
WR_DATA_OUT
BYPASS
REGISTER/FIFO
308
BYPASS
SELECT LOGIC
EN
ACT

Fig. 3

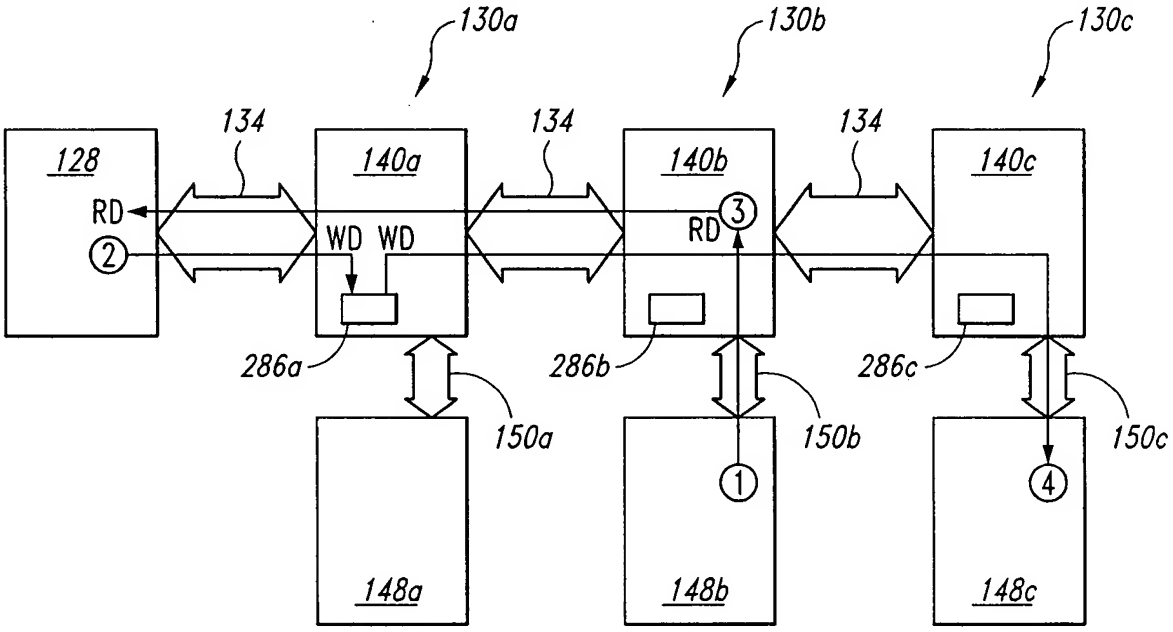

130a
130b
130c
134
134
134
128
140a
140b
140c
RD
2
WD WD
RD
3
286a
286b
286c
150a
150b
150c
1
4
148a
148b
148c

Fig. 4

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450. Alexandria, VA 22313-1450.

June 5, 2007
Date

Sherri A. Phillips

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/773,583	Confirmation No.	: 6732
Applicants	: Douglas A. Larson and Jeffrey J. Cronin		
Filed	: February 5, 2004	Attorney Docket No.	: 501296.01 (30266/US)
Art Unit	: 2188	Customer No.	: 27,076
Examiner	: Duc T. Doan		
Title	: APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM		

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF (37 C.F.R. § 41.37)

Sir:

This brief is in furtherance of the Notice of Appeal filed in this case on April 5, 2007. The fees required under Section 41.20, and any required request for extension of time for filing this brief and fees therefore, are dealt with in the accompanying transmittal letter.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, Micron Technology, Inc., a Delaware Corporation having a principal place of business in Boise, Idaho.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to appellants, the Appellants' legal representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-43.

B. STATUS OF ALL THE CLAIMS

1. Claims canceled: 1-39.
2. Claims withdrawn from consideration but not canceled: None.
3. Claims objected to: None.
4. Claims allowed or confirmed: None.
5. Claims rejected: 36-43.

C. CLAIMS ON APPEAL

The claims on appeal are: 40-43.

IV. STATUS OF AMENDMENTS

Appellants canceled claims 1-4, 11-15, 21-25, and 32-39 after final rejection. (Response dated February 5, 2007 attached hereto as Exhibit B and the Supplemental Response dated June 5, 2007 attached hereto as Exhibit C).

V. SUMMARY OF CLAIMED SUBJECT MATTER

1. Introduction

The present application is directed toward solving the problem of data collisions on a bi-directional data bus in a memory system. In one embodiment shown in Figure 1, a memory system has multiple memory modules 130a-n connected to each other in series and to a memory hub controller 128 via a bi-directional data bus. Data collisions can occur on a bi-directional data bus when a read command is issued before a write command. For example, as read data is heading downstream from a memory device on memory module 130c and write data is simultaneously heading upstream from the memory hub controller 128 to memory module 130n, the read data and the write data would collide. The present application prevents this data collision by using a bypass circuit 286. In one embodiment, the bypass circuit 286 is capable of temporarily storing data passing through a respective memory hub 140. As in the example provided above, as the read data is about to head downstream toward memory module 130b from memory module 130c, the write data is heading upstream from memory module 130a toward memory module 130b. In order to prevent a data collision, the write data is temporarily stored in the bypass circuit 286 in the memory hub 140 of memory module 130b. While the write data is stored in the bypass circuit 286, the read data continues downstream to memory module 130a. Once the read data passes through memory module 130b on its way to memory module 130a, the write data may be recoupled to the bi-directional data bus to continue its way upstream to memory module 130n. Therefore, when a read command is issued before a write command, the corresponding write data can be sent upstream before the read latency of the previously issued read command is complete. *Specification,*. at page 8, lines 12-27, page 10, lines 21-28, page 11, lines 1-22 and Figure 3. (Specification attached hereto as Exhibit D).

2. Claim 40

Claim 40 is directed toward a method for executing read and write commands in a memory system having a bidirectional memory bus. *Specification,* at page 5, lines 15-17. The method of claim 40 includes "issuing a read command to access a first memory location in the memory system" and "before completion of the read command, scheduling a write command to

write data to a second memory location in the memory system." In one embodiment, a read command is issued by the memory hub controller 128 to access a first memory location in a memory system. Before completing the read command, a write command is scheduled by the memory hub controller 128 to write data to a second memory location in the memory system. *Id.* at page 10, lines 21-28.

In addition, claim 40 includes "retrieving read data from the first memory location." In one embodiment, the read data is retrieved from the first memory location. *Id.* at page 10, lines 21-28.

Claim 40 further includes "prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system." In one embodiment, prior to the memory hub controller 128 receiving the read data on the memory bus, the write data corresponding to the write command is provided to the bidirectional memory bus. *Id.* at page 10, lines 27-28 and page 11, line 1.

Claim 40 further includes "in the memory system, bypassing the read data on the bidirectional memory bus." In one embodiment, the read data on the bidirectional memory bus is bypassed while in the memory system when a bypass circuit 286 captures the write data so that read data can be sent to the memory hub controller 128. *Id.* at page 11, lines 1-14. Finally, claim 40 includes "receiving the read data on the bidirectional memory bus from the memory system" and "providing the write data to the bidirectional memory bus." In one embodiment, the read data on the bidirectional memory bus is received by the memory hub controller 128 from the memory system. *Id.* In addition, the write data is provided back to the bidirectional memory bus. *Id.*

VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

The only ground of rejection to be reviewed on appeal is whether claim 40, as well as any claims dependent thereon, are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent Application No. 2005/0105350 to Zimmerman ("Zimmerman"), in view of U.S. Patent No. 6,622,188 to Goodwin et al. ("Goodwin") and further in view of U.S. Patent No. 6,901,494 to Zumkehr et al. ("Zumkehr "). (Office Action dated December 5, 2006 attached hereto as Exhibit A).

VII. ARGUMENTS

I. Claim 40 are Patentable over Zimmerman in view of Goodwin and further in view of Zumkehr

A. The Subject Matter of Claims 40

Claim 40 reads as follows:

> 40. A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:
>
> issuing a read command to access a first memory location in the memory system;
>
> before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;
>
> retrieving read data from the first memory location;
>
> prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;
>
> in the memory system, bypassing the read data on the bidirectional memory bus;
>
> receiving the read data on the bidirectional memory bus from the memory system; and
>
> providing the write data to the bidirectional memory bus.

B. The Subject Matter Disclosed in the Zimmerman Reference

The Zimmerman reference is directed to a memory test mechanism for buffered-memory-module memory subsystems. The Zimmerman reference provides a testing method for evaluating individual memory modules and individual module-to-module memory channels independent of the host and host memory channel. The Zimmerman reference is cited by the

Examiner for disclosing a memory system that includes multiple hub-based memory modules with data paths that interlink the memory module hubs. Although the Zimmerman reference does disclose the memory system described above, it and no other reference cited by the Examiner discloses data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write data.

C. The Subject Matter Disclosed in the Goodwin Reference

The Goodwin reference is directed to an I^2C bus expansion apparatus that permits multiple bus devices of the same group to reside on an I^2C bus in a data processing system. The I^2C bus is a 2-wire bidirectional serial bus for communication between bus devices in a data processing system. The Goodwin reference is cited by the Examiner for disclosing a bidirectional data bus. Although the Goodwin reference discloses a bidirectional data bus, it and no other reference cited by the Examiner discloses data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write data.

D. The Subject Matter Disclosed in the Zumkehr Reference

The Zumkehr reference discloses a RAMBUS control and data bus connecting a RAMBUS memory controller 210 to a translator hub 220, and a SDRAM control and data bus connecting the translator hub 220 to SDRAM memory devices 161. *Zumkehr Specification*, Figure 2. SDRAM devices require write data to be sent with write commands. Therefore in prior systems, write commands were delayed until the write data could be sent from the RAMBUS memory controller to the SDRAM device via the translator hub. Therefore, both the write command and corresponding write data could not be sent until after the read latency of the previous read command was met. The Zumkehr reference, however, teaches the ability to issue a write command without sending the corresponding write data by storing the write command in a write buffer within the translator hub. By being able to send a write command without corresponding write data, the Zumkehr reference teaches the ability to issue a write command after a read command has been issued; however, the Zumkehr reference does not teach

the ability to issue the corresponding write data before the completion of the latency of the previous issued read command. *Zumkehr Specification*, column 4, lines 45-68 – column 5, lines 1-13.

In Figure 5A, the Zumkehr reference discloses a timing diagram of a memory system where the translator hub does not include a write buffer and Figure 5B shows a timing diagram where the translator hub does include a write buffer. In Figure 5A, a write command following a read command is delayed by a period corresponding to the read latency of the previous read command. In contrast, Figure 5B, which includes a write buffer in the translator hub, shows that a new write command 520B following a read command 501B can be issued before the read latency of the previously issued read command 501B is met. Once the new write command 520B is received in the translator hub, *a previous* write command 522B and corresponding write data 525B already stored in the translator hub are sent to the memory devices. However, the write data 527B associated with the new write command 520B remains in the memory controller and cannot be issued until *after* the read latency of the previously issued read command 501B is met. *Zumkehr Specification*, column 5, lines 39-44, column 6, lines 53-67 – column 7, lines 1-49 and Figures 5A and 5B. Therefore, the Zumkehr reference does not disclose or fairly suggest data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write.

E. Summary of the Rejection

The final rejection dated December 5, 2006 rejects claim 40 as being unpatentable under 35 U.S.C. § 103(a) over Zimmerman, in view of Goodwin, and further in view of Zumkehr.

In the Office Action, the Examiner rejected claim 40 under the same rationale as cancelled claim 1. *Office Action*, page 5, line 7 and page 7, lines 8-13, respectively. Under claim 1, the Examiner contends that Zumkehr discloses a write bypass circuit coupled to a direct data path and temporarily storing write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred

through the direct data path. In particular, the Examiner contends that the multiplexer or the write buffer in Figure 6 of the Zumkehr reference is analogous to the write bypass circuit of claim 1.

Claim 40 is patentably distinct from claim 1. Cancelled claim 1 disclosed a write bypass circuit coupled to a bidirectional data path capable of temporarily storing write data to allow read data to pass through the bidirectional data path and then recoupling the stored write data to the data path. Therefore, write data and read data could be on the bidirectional data path at the same time, moving in opposite directions and still avoid a data collision. Claim 1 did not require that the write command and corresponding write data be issued before completion of the read command. However, method claim 40 requires scheduling a write command to write data before completion of a previously issued read command.

It appears that the Examiner contends that the Zumkehr reference discloses a method of bypassing write data regardless of whether the latency of a previous read command is met. The Appellants contend that the Zumkehr reference does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued followed by a write command and corresponding write data, when the write command and corresponding write data are issued before the read latency is met.

F. The Zimmerman, Goodman, and Zumkehr References, in Combination or by Themselves, Do Not Disclose All of the Limitations of Claim 40

The Zumkehr reference was cited by the Examiner for disclosing a method of bypassing the read data on the bidirectional memory bus of claim 40. The Examiner contends that the multiplexer 650 or the write buffers 330 within the translator hub 220 have the capability of storing write data in order to prevent data collisions on a bidirectional data bus similar to the bypass circuit of the present application. The Zumkehr reference, however, does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued, and before the read latency is met, issuing a write command and corresponding write.

As described above, the Zumkehr reference discloses a bus connecting a RAMBUS memory controller 210 to a translator hub 220, and an SDRAM bus connecting the translator hub 220 to SDRAM memory devices 161. The write buffer in the translator hub is capable of receiving a write command at a different time than the corresponding write data and sending the write command and corresponding write data to the SDRAM devices. *Id.* at column 5, lines 39-44 and Figure 5B. This improves the performance of the data transfer, because the write command can be issued from the memory controller without requiring the corresponding write data to be sent from the memory controller one clock cycle later. For example, a situation in which the corresponding write data can not be sent with the write command exits when a read command has already been issued. The write data must wait for the read latency of the previously issued read command to be met before it can be transferred to the translator hub. *Id.* at column 7, lines 18-20 stating "the RAMBUS memory controller 210 defers write data transfer on a write command until the read latency of a previous read command is met". Once the translator hub receives the new write command, *a previously issued* write command and corresponding write data that were stored in the translator hub *before* the read command was issued may be sent to the memory devices before the read latency of the read command is complete. *See, Id.* at column 6, lines 53-67 – column 7, lines 1-49, and Figure 5B. Therefore, only the write data that was already issued and located on the translator hub may go onto the data bus after a subsequent read command is issued. If write data were issued from the memory hub after a read command was issued, there would be a collision on the RAMBUS data bus as the read data is heading downstream to the memory controller and the write data is heading upstream to the translator hub. Therefore, the Zumkehr reference does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued, but before the read latency is met, issuing a write command *and corresponding write data*.. Neither the Zimmerman reference nor the Goodman reference make up for the deficiencies of the Zumkehr reference.

Turning now to the claims, the Zimmerman, Goodman, and Zumkehr references, in combination or alone, do not disclose all the limitations of claim 40. A claim

rejected under 35 U.S.C. § 103(a) must teach or suggest all of the claim limitations. M.P.E.P. 706.02(j).

Method claim 40 requires, in part, issuing a read command, *before completion of the read command*, scheduling a write command, retrieving the read data, but prior to receiving the read data from the memory system, providing write data corresponding to the write command to the bidirectional memory bus, and in the memory system, bypassing the read data on the bidirectional memory bus. As alluded to above, the Zumkehr reference fails to disclose or suggest the above limitation. Rather, the Zumkehr reference waits for the read latency of a read command to end before issuing the write data that corresponds to a write command issued after the read command. In contrast, method claim 40 requires providing write data to the bidirectional memory bus prior to receiving the read data from the memory system. Therefore, claim 40 is allowable over the Zumkehr reference.

Neither the Zimmerman reference nor the Goodwin reference make up for the deficiencies in the Zumkehr reference discussed above. In fact, the Examiner explicitly admits in the Final Office Action dated December 5, 2006 that neither the Zimmerman reference nor the Goodwin reference disclose a bypath data path. *Office Action*, page 4, line 6.

For all of the reasons explained above, neither the Zumkehr reference, the Zimmerman reference, nor the Goodwin reference, in combination or by themselves, disclose or fairly suggest all elements of claim 40 in the present application. Therefore, the rejection of claim 40, as well as claims dependent thereon, should be reversed.

VIII. CLAIMS APPENDIX

The text of the claims involved in the appeal are:

40. A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

IX. EVIDENCE APPENDIX

1. Office Action dated December 5, 2006 and prior art cited therein attached hereto as Exhibit A.

2. Response dated February 5, 2007 attached hereto as Exhibit B.

3. Supplemental Response dated June 5, 2007 attached hereto as Exhibit C.

4. Applicants' Specification, filed February 5, 2004 attached hereto as Exhibit D.

X. RELATED PROCEEDINGS APPENDIX

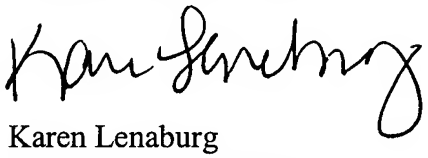
None.

XI. CONCLUSION

For all of the reasons stated above, the rejection of claims 40-43 should be reversed.

Respectfully submitted,

DORSEY & WHITNEY LLP



Karen Lenaburg
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KL:sp

Enclosures:
Postcard
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Fee Transmittal (+ copy)
Appeal Brief Transmittal (+copy)

1420 Fifth Avenue, Suite 3400
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Tel: (206) 903-2399
Fax: (206) 903-8820

IDS REFERENCES

☒ FOR Exhibit A

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,583	02/05/2004	Douglas A. Larson	501296.01 (30266/US)	6732

7590 12/05/2006

Kimton N. Eng, Esq.
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1420 Fifth Avenue, Suite 3400
Seattle, WA 98101

EXAMINER	
DOAN, DUC T	
ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

FINAL REJECTION

2 mo. Response Due: February 5, 2007
3 mo. Response Due: March 5, 2007
Notice of Appeal Due: June 5, 2007
(6 mo. period ends/3 mo. ext. of time required - will go abandoned)

AJS

Office Action Summary	Application No.	Applicant(s)	
	10/773,583	LARSON ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,11-15,21-25 and 32-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,11-15,21-25 and 32-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 6/19/2006
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-43 have been presented for examination in this application. In response to the last office action, claims 1-3,11-13,21-23,32,36,40 have been amended, claims 5-10,16-20,26-31 have been canceled. As the result, claims 1-4,11-15,21-25,32-43 are pending in this application.

Claims 1-4,11-15,21-25,32-43 are rejected.

All rejections and objections not explicitly repeated below are withdrawn.

Applicant's amendments/remarks filed 9/19/06 have been fully considered but they are mooted in view of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

The information disclosure statements filed 9/19/06 fails to comply with the provisions of 37 CFR 1.97, 1.98 because it does not list any prior art to be considered. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,4,11,14-15,21,24-25,32-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350), in view of Goodwin et al (US 6622188), and further in view of Zumkehr (US 6901494).

As in claim 1, Zimmerman describes a memory hub for a hub-based memory module (Zimmerman's Fig 2: MMB, paragraph 17), comprising: first and second link interfaces for coupling to respective data busses; a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces (Zimmerman's Fig 2, links 112 on both sides of MMB; paragraphs 15);

Zimmerman does not disclose the claim's aspect of a bidirectional data bus operable to transfer both read and write data. However, Goodwin discloses a mechanism in which multiple memory devices are connected to a bidirectional bus as depicts in Goodwin's Fig 2: Expansion devices. It would have been obvious to one of ordinary skill in the art at the time of invention to include bi directional bus mechanism as suggested by Goodwin in Zimmerman's system thereby further allow read and write data in expansion devices such as memory devices to be transferred effectively over the same bidirectional data bus (Goodwin's column 1 lines 10-35). Zimmerman

discloses first and second link interfaces for coupling to respective portions of the bus the portion of the data bus (i.e Host side and downstream sides of the links 132, 142, each segment represent a portion of the data bus). Goodwin further discloses the expansion memory #216 having the direct data path (SCL 236 through which data is transferred between the first (i.e link to expansion memory 215) and second link (i.e link to expansion memory 218) interfaces, Zimmerman and Goodwin do not expressly disclose the claim's detail of bypath data path. However, Zumkehr's discloses a bypath data path having a write bypass circuit coupled to the direct data path and temporarily store the write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred through the direct data path (Zumkehr's Fig 7 #730 discloses the circuits in the translator hub providing a direct data path, in which the write data received by the translator hub (Fig 2: #220) is immediately and directly forwarding to the downstream device; Zumkehr's Fig 6 discloses a multiplexer (i.e write by pass circuit) that allowing temporary stored the write data while allowing the read data to be transferred through the direct data path, directly to the upstream device; subsequently the multiplexer recouple the stored write data and sending to the downstream device; Zumkehr's column 7 lines 17-23 discloses the write command received by the translator circuit must be delayed and allowing the read command to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory controller hub circuits and methods as suggested by Zumkehr in Zimmerman's system to allow transferring read data while

temporary storing write data, thereby resulting in more efficiently usage of the memory bus in the system (Zumkehr's column 6 lines 35-60; read and write data transferring through the same bidirectional data bus Fig 3: #350 data signals).

As in claim 4, Zimmerman's Fig 5 describes a memory device interface coupled to the data path, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

Claims 11,21,32,36 rejected based on the same rationale as in the rejection of claim 1.

Claims 14,24 rejected based on the same rationale as in the rejection of claim 4.

As in claim 15, Zimmerman discloses a memory controller (Fig 2: MMB) coupled to a data path through a memory controller bus (Zimmerman's Fig 2: 112); and further coupled to at least one of the plurality of memory devices through a memory device bus (MMB couples to memory device DRAM obviously vie DRAM memory device bus), a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device (Zimmerman's paragraph 15 discloses the buffered memory modules/controller logic to store the memory requests and to store the memory data receiving from the host).

Claim 21 rejected based on the same rationale as in the rejection of claim 1.Zimmerman's Fig 1 further discloses a processor (Zimmerman's Fig 1: #20) and processor bus connecting the processor to the system controller (Zimmerman's Fig 1: #30 MCH), which obviously having associating ports connecting to peripheral devices such as memory data storage devices

(Zimmerman's Fig 2: DRAM); a memory module (Zimmerman's Fig 3a) comprising memory hub (Fig 2: MMB). The remaining limitation of claim 21 is rejected based on the same rationale as of claim 1.

Claim 25 rejected based on the same rationale as of claim 15.

As in claim 33, Zumkehr's column 7 lines 17-23 discloses the write command received by the translator circuit must be delayed and allowing the read command to be issued earlier and, to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals.

As in claim 34, Zumkehr describes translator circuit to translate a write command to an sdram write command for the memory device, in addition to the FIFO queue for other write commands being received (Zumkehr's column 5 lines 5-12).

As in claim 35, Zimmerman discloses wherein the memory system includes a plurality of memory modules coupled in series on the memory bus (Zimmerman's Fig 2 DRAM memory modules #120, #130 in serial on the memory bus), and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed (Zimmrman's Fig 2 discloses writing to memory module #130 located downstream from memory module #120 in which the read data is accessed by the host #110).

Claim 37 rejected based on the same rationale of claim 33.

As in claim 38, Zumkehr's describes the write buffer to temporary store write data request (zumkerhr's Fig 3: #330).

As in claim 39, the claim recites wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus. Zumkehr further describes the write buffer in MMB is provided to temporary store data from host and thus decoupling the host to handle another accessing data on the memory bus (Zumkehr's Fig 5)

Claim 40 rejected based on the same rationale as of claim 1. Zimmerman further discloses a memory system with multiple buffered memory modules; each memory buffer module can buffer write and read command issued from the host (Fig 2: #110). Thus the host can continue issuing commands to these buffered memory modules in concurrently manner, that is the read command can be issued to memory module Fig 2: #130 before issuing the write command to memory module Fig 2: #120.

As in claim 41, the claim rejected based on the same rationale as of claim 40. Zumkehr's column 7 lines 17-23 further discloses the write command received by the translator circuit must be delayed for a time period and allowing the read command to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals. Therefore the collision on the bi-direction data bus can be averted.

As in claims 42-43, Zumkehr discloses the write data is stored temporary in Fig 3: #330 to avoid the collision with the read data receiving from bi-directional data signal Fig 2: 350's

data signals (claim 42); wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus (claim 43; Zumkehr discloses a FIFO to temporary store write commands (i.e sending the write data of the first write command to at least one memory module, receiving read command, storing the data of the second write command in the FIFO before decoupling and allowing the data of a read travels through the memory bus (from Fig 3: #350 data signals to the host, Fig 3: #310 data signal).

Claims 2-3,12-13,22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350), in view of Goodwin et al (US 6622188), Zumkehr (US 6901494) as applied to claims 1,11,21 respectively, and in view of Garcia et al (US 6782435).

As in claim 2, although Zumkehr's Fig 6: #650 discloses the multiplexer providing the directly data path (read data) and the bypass data path (write data), Zumkehr does not expressly disclose the claim's detail of the multiplexer. However, Garcia's Fig 2 teaches in detail a multiplex circuit comprises a multiplexer, a bypass selection signal, and a register to temporary store write data being received. It would have been obvious to one of ordinary skill in the art at the time of invention to include the temporary storage and the multiplexer circuits as suggested by Garcia in Zimmerman's system to temporary reordering the transmitting data thereby allowing accessing memory device with minimum latency and maximizing the throughput of he overall system (Garcia's column 1, lines 48-62).

As in claims 3, the claim recite wherein the write bypass circuit further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register. The claim rejected based on the same rationale as in the rejection of claim 2.

Claims 12,22 rejected based on the same rationale as of claim 2.

Claims 13,23 rejected based on the same rationale as of claim 3.

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

Regarding remarks on pages 11-12 for the Zimmerman's expressly teaching of the bidirectional data bus. It's mooted in view of the new reference Goodwin et al, new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

Regarding the remark on pages 12-17, Applicant contends that Zumkehr does not provide a direct data path for the write data to be provided to the down stream device (i.e the sdram device). Examiner respectfully disagrees. Zumkehr's Fig 6 discloses a multiplexer in the translator hub that provides a data path directly to the downstream device, when it received the write data sent from the host's Fig 3: #210; receiving at its buffer Zumker's Fig 3: #330 and sending directly to down stream devices Fig 3: #161. Examiner notes that the same mechanism is

disclosed in specification's Fig 3, that is host's data is received at a receiving buffer Fig 3: 302 and subsequently it is sent directly to down stream device.

Applicant contends that Zumkehr's buffering circuits do not provide avoiding the data collision between data heading the opposite directions on the bidirectional data paths. Examiner respectfully disagrees, Zumkehr discloses write buffers that temporary store write data of write requests so that the read data of the read command can be sent on the opposite direction toward the host on the same bidirectional bus, Fig 3: #350 data signals. Thus the write data toward the down stream device is temporary stored, delay and avoids the collision with the read data traveling in opposite direction on the same bidirectional data bus (see Zumkehr's column 6 lines 22-30).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
11/29/06

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 501296.01 (30266/US)	APPLICATION NO. 10/773,583
INFORMATION DISCLOSURE STATEMENT *(Use additional sheets if necessary)*		APPLICANT(S) Douglas A. Larson and Jeffrey J. Cronin	
		FILING DATE February 5, 2004	GROUP ART UNIT 2188

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
DD	AA	6,324,485 B1	11/27/01	Ellis	702	117	
	AB	6,526,483 B1	02/25/03	Cho et al.	711	154	
	AC	6,636,912 B2	10/21/03	Ajanovic et al.	710	105	
	AD	2003/0005344 A1	01/02/03	Bhamidipati et al.	713	400	
	AE	2003/0156581 A1	08/21/03	Osborne	370	389	
	AF	2003/0229762 A1	12/11/03	Maiyuran et al.	711	137	
	AG	2005/0015426 A1	01/20/05	Woodruff et al.	709	200	
	AH	2005/0149603 A1	07/07/05	DeSota et al.	709	200	
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AM							
	AN							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

DD	AO	Rambus, Inc., "Direct Rambus™ Technology Disclosure", October 1997. pp. 1-16.
	AP	
	AQ	

EXAMINER	DATE CONSIDERED
Luc Doan	11/28/06

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

Notice of References Cited	Application/Control No. 10/773,583	Applicant(s)/Patent Under Reexamination LARSON ET AL.	
	Examiner Duc T. Doan	Art Unit 2188	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,622,188	09-2003	Goodwin et al.	710/105
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

IDS REFERENCES

☐ ~~FOR~~ Exhibit B.

RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE - EXAMINING GROUP 2100

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

February 7, 2007 _____
Date Sherri A. Phillips

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/773,583	Confirmation No.	: 6732
Applicants	: Douglas A. Larson and Jeffrey J. Cronin		
Filed	: February 5, 2004	Attorney Docket No.	: 501296.01 (30266/US)
Art Unit	: 2188	Customer No.	: 27,076
Examiner	: Duc T. Doan		
Title	: APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 C.F.R. § 1.116

Sir:

Applicants acknowledge receipt of the Office Action dated December 5, 2006. Please amend the above-captioned patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks begin on page 7 of this paper.

Amendments to the Specification:

Please replace paragraph [23] with the following amended paragraph:

--In operation, WR_DATA_IN received by the data bypass circuit 300 is driven through the input buffer 302 and is provided to the first input of the multiplexer 306. The WR_DATA_IN is also saved in the bypass register/FIFO 304. In response to an inactive ACT signal, an active EN signal is generated by the bypass select logic 308. The active EN signal enables output by the input/output buffer 310 and couples the output of the input buffer 302 to the input of the input/output buffer 310 through the multiplexer 306. As a result, the WR_DATA_IN is provided directly to the input of the input/output buffer 310 and the WR_DATA_IN is provided through the data bypass circuit 300 without any bypass. However, in response to an active ACT signal, the bypass select logic 308 generates an inactive EN signal, disabling the output function of the input/output buffer 310 and placing its output in a high-impedance state. Additionally, the inactive EN signal couples the input of the input/output buffer 310 to the output of the bypass register/FIFO 304. In this manner, the WR_DATA_IN is received by the data bypass circuit 300, stored by the bypass register/FIFO ~~306~~ 304, and applied to the input of the input/output buffer 310. However, due to the inactive state of the EN signal, the WR_DATA_IN is not provided as output data WR_DATA_OUT by the input/output buffer 310. As a result, the WR_DATA_IN is held in a bypass state until the ACT signal becomes inactive, at which time, the EN signal become active again, enabling the input/output buffer 310 to provide the WR_DATA_IN as WR_DATA_OUT data. The multiplexer 306 is also switched back to coupling the output of the input buffer 302 directly to the input of the input/output buffer 310 to allow WR_DATA_IN to pass through the data bypass circuit unhindered.--

Please replace paragraph [25] with the following amended paragraph:

--In Figure 4, it is assumed that the memory hub controller 128 has just issued read and write commands, with the read command sequenced prior to the write command. The read command is directed to the memory module 130b and the write command is directed to the memory module 130c. That is, the memory module to which data will be written is further downstream than the memory module from which data is read. In response to the read command, the memory hub 140b begins retrieving the read data (RD) from the memory device 148b, as indicated in Figure 4 by the "(1)". With the read command issued, the write command

is then initiated, and the write data (WD) is provided onto the high-speed link 134. However, since the memory hub controller 128 is expecting the RD to be returned from the memory module 130b, the memory hub 140a is directed to capture the WD in its data bypass circuit 286a. As a result, the ~~memory hub~~ data bypass circuit 286a captures the WD to clear the high-speed link 134, as indicated in Figure 4 by the "(2)", for the RD to be returned to the memory hub controller 128. When the memory hub 140b has retrieved the RD from the memory device 148b, and has indication from the memory hub 140a that the WD has been successfully captured by the data bypass circuit 286a, the RD is then provided to the memory hub controller 128 through the high-speed link 134, as indicated in Figure 4 by the "(3)" to complete the read request. Upon the RD passing through the memory hub 140a on its way to the memory hub controller 128, the memory hub 140a releases the WD from the data bypass circuit 286a to continue its way to the memory hub 140c. The WD is provided to the memory hub 140c through the high-speed link, which is now clear between the memory hub 140a and 140c. Upon reaching the memory hub 140c, the WD is written in the memory device 148c, as shown in Figure 4 by the "(4)".--

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 1-4, 11-15 and 21-25, and amend claims 32 and 40 as follows:

Listing of Claims:

1-31. (Canceled)

32. (Currently Amended) A method for writing data to a memory location in a memory system coupled to a bidirectional memory bus transmitting both read and write data, comprising:

~~accessing read data in~~ issuing a read command to the memory system;

providing a write command and corresponding write data to the memory system on the bidirectional memory bus, after issuing the read command;

coupling the write data to a register in the memory system for temporary storage of the write data to allow the read data to be returned on the bidirectional data bus after the write data is provided to the same and before the write data has been written;

coupling the read data to the bidirectional memory bus and providing the read data for reading;

coupling the write data stored in the register to the bidirectional memory bus; and

writing the write data to the memory location.

33. (Original) The method of claim 32, further comprising issuing a read command to the memory system prior to issuing a write command to the memory system.

34. (Original) The method of claim 32 wherein providing the write data to the memory system comprises providing the write data through at least one memory module of the memory system prior to coupling the write data to the register.

35. (Original) The method of claim 32 wherein the memory system includes a plurality of memory modules coupled in series on the memory bus, and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed.

36. (Previously Presented) A method for executing memory commands in a memory system having a memory bus on which both read and write data can be coupled, the method comprising:

issuing a read command to the memory system;

issuing a write command to a memory location in the memory system and providing write data for the write command to the memory bus of the memory system after issuing the read command;

accessing read data in the memory system;

in the memory system, decoupling the write data from the memory bus;

receiving the read data on the memory bus from the memory system;

recoupling the write data to the memory bus; and

resuming the write command to the memory location.

37. (Original) The method of claim 36 wherein issuing the read command to the memory system precedes issuing the write command to the memory system.

38. (Original) The method of claim 36, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

39. (Original) The method of claim 36 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

40. (Currently Amended) A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. (Original) The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. (Original) The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. (Original) The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

REMARKS

The specification has been amended in order to resolve obvious errors. No new matter was added.

The Applicants would like to thank the Examiner for the telephone interview conducted on February 1, 2007. During the interview the Applicants stated that the write buffer in the Zumkehr patent, Patent No. 6,901,494, does not disclose a bypass data path having a write bypass circuit coupled to a direct data pass operable to temporarily store the write data to allow read data to be transferred through the direct data path. The Examiner did not agree. The Examiner suggested that the Applicants draft an argument for his Supervisor to review. The Applicants would like to thank the Examiner and his Supervisor for the opportunity to have the argument reviewed by the Examiner's Supervisor.

After the interview, Applicants' attorney spent a great deal of time studying the Zumkehr patent and now has a better understanding of the Examiner's position. Applicants admit that there are some similarities between subject matter disclosed in the present application and the Zumkehr patent for situations in which the write data is passed from the controller 210 to the translator hub 220 *before* a read command is applied to the hub 220. For example in Zumkehr, write data is passed from the controller 210 to the translator hub 220 before a read command is passed from the controller 210 to the translator hub 220 and from the translator hub 220 to the appropriate memory device 161. The read data is then passed from the memory device 161 to the translator hub 220. A write command corresponding to the previous write data is then sent from the controller 210 to the translator hub 220. During the time the read data is being sent from the translator hub 220 to the controller 210, the write data also is sent from the translator hub 220 to the appropriate memory device 161. Therefore, data is being transferred on the bus at the same time. *Zumkehr Specification*, Figure 5B and column 6, lines 53-67 - column 7, lines 1-49.

On the other hand, there are differences that are significant for situations where, as in applicants' system, the write command and corresponding write data are output from a controller *after* the read command are output from the controller. In the Zumkehr system, when a read command is issued to the memory system before a write command and corresponding write data are issued to the memory system, the controller 210 defers the transfer of the write data from the controller 210 to the translator hub 220 until the read latency is met. *Zumkehr*

specification, column 7, lines 15-20 and Figure 5B. The disclosed system, however, does not require that the read latency be met before transferring the write command and corresponding write data from the controller to the memory system. Rather, the write command and corresponding write data may be provided to the memory system after the read command is issued to the memory system. This means that read data will be going in one direction to the controller and write data will be going in the opposite direction to a memory device at the same time. In order to prevent a collision on the data bus, the write data is decoupled from the bidirectional data bus by the bypass register. Once the read data has passed the bypass register, the write data is recoupled to the bidirectional data bus. Because the Zumkehr patent requires the write data to be already stored in the hub before a read command is issued, it does not meet all of the requirements for the method claims in the present application.

The Applicants propose canceling the apparatus claims, 1-4, 11-15, and 21-25 in the present application. The Applicants further propose filing a continuation application to prosecute amended apparatus claims separately from the method claims of the current application. In addition, the Applicants propose amending independent method claim 32 in the present application so that it has limitations similar to those already included in independent method claims 36 and 40, that the read command is issued to the memory system before the write data is provided to the memory system.

Upon the Examiner's acceptance of the proposed changes, all of the claims remaining in the application are clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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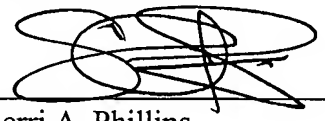
IDS REFERENCES

☐ ~~FOR~~ Exhibit E

RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE - EXAMINING GROUP 2100

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

June 5, 2007 

Date Sherri A. Phillips

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/773,583	Confirmation No.	: 6732
Applicants	: Douglas A. Larson and Jeffrey J. Cronin		
Filed	: February 5, 2004	Attorney Docket No.:	501296.01 (30266/US)
Art Unit	: 2188	Customer No.	: 27,076
Examiner	: Duc T. Doan		
Title	: APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL RESPONSE UNDER 37 C.F.R. § 1.116

Sir:

Applicants acknowledge receipt of the Office Action dated December 5, 2006. Further to the response filed February 7, 2007, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 4 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 32-39.

Listing of Claims:

1-39. (Canceled)

40. (Previously Presented) A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. (Original) The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. (Original) The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. (Original) The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

REMARKS

Applicants filed a Notice of Appeal on April 5, 2007. Applicants acknowledge receipt of the Office Action dated December 5, 2006, and further to the response filed February 7, 2007, request the cancellation of claims 32-39.

Respectfully submitted,

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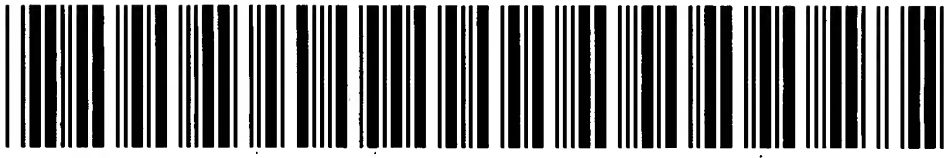
IDS REFERENCES



☐ ~~FOR~~ Exhibit D

APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM

TECHNICAL FIELD

The present invention relates to memory systems, and more particularly, to memory modules having a data bypass for preventing data collision on a bi-direction data bus.

BACKGROUND OF THE INVENTION

Computer systems use memory devices, such as dynamic random access memory ("DRAM") devices, to store data that are accessed by a processor. These memory devices are normally used as system memory in a computer system. In a typical computer system, the processor communicates with the system memory through a processor bus and a memory controller. The memory devices of the system memory, typically arranged in memory modules having multiple memory devices, are coupled through a memory bus to the memory controller. The processor issues a memory request, which includes a memory command, such as a read command, and an address designating the location from which data or instructions are to be read. The memory controller uses the command and address to generate appropriate command signals as well as row and column addresses, which are applied to the system memory through the memory bus. In response to the commands and addresses, data are transferred between the system memory and the processor. The memory controller is often part of a system controller, which also includes bus bridge circuitry for coupling the processor bus to an expansion bus, such as a PCI bus.

In memory systems, high data bandwidth is desirable. Generally, bandwidth limitations are not related to the memory controllers since the memory controllers sequence data to and from the system memory as fast as the memory devices allow. One approach that has been taken to increase bandwidth is to increase the speed of the memory data bus coupling the memory controller to the memory devices. Thus, the same amount of

information can be moved over the memory data bus in less time. However, despite increasing memory data bus speeds, a corresponding increase in bandwidth does not result. One reason for the non-linear relationship between data bus speed and bandwidth is the hardware limitations within the memory devices themselves. That is, the memory controller has to schedule all memory commands to the memory devices such that the hardware limitations are honored. Although these hardware limitations can be reduced to some degree through the design of the memory device, a compromise must be made because reducing the hardware limitations typically adds cost, power, and/or size to the memory devices, all of which are undesirable alternatives. Thus, given these constraints, although it is easy for memory devices to move "well-behaved" traffic at ever increasing rates, for example, sequel traffic to the same page of a memory device, it is much more difficult for the memory devices to resolve "badly-behaved traffic," such as bouncing between different pages or banks of the memory device. As a result, the increase in memory data bus bandwidth does not yield a corresponding increase in information bandwidth.

In addition to the limited bandwidth between processors and memory devices, the performance of computer systems is also limited by latency problems that increase the time required to read data from system memory devices. More specifically, when a memory device read command is coupled to a system memory device, such as a synchronous DRAM ("SDRAM") device, the read data are output from the SDRAM device only after a delay of several clock periods. Therefore, although SDRAM devices can synchronously output burst data at a high data rate, the delay in initially providing the data can significantly slow the operating speed of a computer system using such SDRAM devices. Increasing the memory data bus speed can be used to help alleviate the latency issue. However, as with bandwidth, the increase in memory data bus speeds do not yield a linear reduction of latency, for essentially the same reasons previously discussed.

Although increasing memory data bus speed has, to some degree, been successful in increasing bandwidth and reducing latency, other issues are raised by this

approach. For example, as the speed of the memory data bus increases, loading on the memory bus needs to be decreased in order to maintain signal integrity since traditionally, there has only been wire between the memory controller and the memory slots into which the memory modules are plugged. Several approaches have been taken to accommodate the increase in memory data bus speed. For example, reducing the number of memory slots, adding buffer circuits on a memory module in order to provide sufficient fanout of control signals to the memory devices on the memory module, and providing multiple memory device interfaces on the memory module since there are too few memory module connectors on a single memory device interface. The effectiveness of these conventional approaches are, however, limited. A reason why these techniques were used in the past is that it was cost-effective to do so. However, when only one memory module can be plugged in per interface, it becomes too costly to add a separate memory interface for each required memory slot. In other words, it pushes the system controllers package out of the commodity range and into the boutique range, thereby, greatly adding cost.

One recent approach that allows for increased memory data bus speed in a cost effective manner is the use of multiple memory devices coupled to the processor through a memory hub. In a memory hub architecture, or a hub-based memory sub-system, a system controller or memory controller is coupled over a high speed bi-directional or unidirectional memory controller/hub interface to several memory modules. Typically, the memory modules are coupled in a point-to-point or daisy chain architecture such that the memory modules are connected one to another in series. Thus, the memory controller is coupled to a first memory module, with the first memory module connected to a second memory module, and the second memory module coupled to a third memory module, and so on in a daisy chain fashion.

Each memory module includes a memory hub that is coupled to the memory controller/hub interface and a number of memory devices on the module, with the memory hubs efficiently routing memory requests and responses between the controller and the memory devices over the memory controller/hub interface. Computer systems employing

this architecture can use a high-speed memory data bus since signal integrity can be maintained on the memory data bus. Moreover, this architecture also provides for easy expansion of the system memory without concern for degradation in signal quality as more memory modules are added, such as occurs in conventional memory bus architectures.

Although computer systems using memory hubs may provide superior performance, they may often fail to operate at optimum efficiency for a variety of reasons. One such reason is the issue of managing data collision between data flowing to and from the memory controller through the memory hubs. In conventional memory controllers, one approach taken to avoid data collision is to delay the execution of one memory command until the completion of another memory command. For example, with a conventional memory controller, a write command issued after a read command is not allowed to begin until the read command is nearly completed in order to avoid the read (i.e., inbound) data colliding with the write (i.e., outbound) data on the memory bus. However, forcing the write command to wait effectively reduces bandwidth, which is inconsistent with what is typically desired in a memory system.

SUMMARY OF THE INVENTION

One aspect of the present invention is directed to a memory hub having a data bypass circuit. The memory hub includes first and second link interfaces for coupling to respective data busses, a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces. The memory hub further includes a write bypass circuit coupled to the data path for coupling write data on the data path and temporarily storing the write data to allow read data to be transferred through the data path while the write data is temporarily stored. In another aspect of the invention, a method for writing data to a memory location in a memory system coupled to a memory bus is provided. The method includes accessing read data in the memory system, providing write data to the memory system on the memory bus, and coupling the write data to a register for temporary storage of the write data. While the data is temporarily stored,

the read data is coupled from the memory bus and provided for reading. The write data is recoupled to the memory bus and written to the memory location.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a computer system having memory modules in a memory hub architecture in which embodiments of the present invention can be implemented.

Figure 2 is a partial block diagram of a memory hub according to an embodiment of the present invention for use with the memory modules of Figure 1.

Figure 3 is a block diagram of a data bypass circuit for the memory hub of Figure 2 according to an embodiment of the present invention.

Figure 4 is a block diagram illustrating the operation of the data bypass circuit of Figure 3 for a computer system having the memory hub architecture of Figure 1 and the memory hub of Figure 2.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention are directed to a memory hub having bypass circuitry that provides data bypass for a bi-directional data bus in a hub-based memory sub-system. Certain details are set forth below to provide a sufficient understanding of various embodiments of the invention. However, it will be clear to one skilled in the art that the invention may be practiced without these particular details. In other instances, well-known circuits, control signals, and timing protocols have not been shown in detail in order to avoid unnecessarily obscuring the invention.

Figure 1 illustrates a computer system 100 according to one embodiment of the present invention. The computer system 100 includes a processor 104 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. The processor 104 includes a processor bus 106 that normally includes an address bus, a control bus, and a data bus. The processor bus 106 is typically

coupled to cache memory 108. Typically, the cache memory 108 is provided by a static random access memory ("SRAM"). The processor bus 106 is also coupled to a system controller 110, which is sometimes referred to as a bus bridge.

The system controller 110 serves as a communications path to the processor 104 for a variety of other components. For example, as shown in Figure 1, the system controller 110 includes a graphics port that is typically coupled to a graphics controller 112. The graphics controller is typically coupled to a video terminal 114, such as a video display. The system controller 110 is also coupled to one or more input devices 118, such as a keyboard or a mouse, to allow an operator to interface with the computer system 100. Typically, the computer system 100 also includes one or more output devices 120, such as a printer, coupled to the processor 104 through the system controller 110. One or more data storage devices 124 are also typically coupled to the processor 104 through the system controller 110 to allow the processor 104 to store data or retrieve data from internal or external storage media (not shown). Examples of typical storage devices 124 include hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs).

The system controller 110 includes a memory hub controller 128 that is coupled to memory hubs 140 of several memory modules 130a, 130b, 130c, . . . 130n. The memory modules 130 serve as system memory for the computer system 100, and are preferably coupled to the memory hub controller 128 through a high-speed bi-directional memory controller/hub interface 134. The memory modules 130 are shown coupled to the memory hub controller 128 in a point-to-point arrangement in which the memory controller/hub interface 134 is coupled through the memory hubs 140 of the memory modules 130. That is, the memory controller/hub interface 134 is a bi-directional bus that couples the memory hubs 140 in series. Thus, information on the memory controller/hub interface 134 must travel through the memory hubs 140 of "upstream" memory modules 130 to reach a "downstream" destination. For example, with specific reference to Figure 1, information transmitted from the memory hub controller 128 to the memory hub 140 of the

memory module 130c will pass through the memory hubs 140 of the memory modules 130a and 130b.

It will be appreciated, however, that topologies other than the point-to-point arrangement of Figure 1 may also be used. For example, a coupling arrangement may be used in which a separate high-speed link (not shown) is used to couple each of the memory modules 130 to the memory hub controller 128. A switching topology may also be used in which the memory hub controller 128 is selectively coupled to each of the memory modules 130 through a switch (not shown). Other topologies that may be used will be apparent to one skilled in the art. Additionally, the memory controller/hub interface 134 coupling the memory modules to the memory hub controller may be an electrical or optical communication path. However, other types of communications paths can be used for the memory controller/hub interface 134 as well. In the event the memory controller/hub interface 134 is implemented as an optical communication path, the optical communication path may be in the form of one or more optical fibers. In such case, the memory hub controller 128 and the memory modules will include an optical input/output port or separate input and output ports coupled to the optical communication path, as well known in the art.

The memory hubs 140 control access to memory devices 148 of the respective memory module 130. In Figure 1, the memory devices are illustrated as synchronous dynamic random access memory ("SDRAM") devices. However, memory devices other than SDRAM devices may also be used. As also shown in Figure 1, the memory hub is coupled to four sets of memory devices 148 through a respective memory bus 150. Each of the sets includes four memory devices 148 for a total of 20 memory devices 148 for each memory module 130. The memory busses 150 normally include a control bus, an address bus, and a data bus, as known in the art. However, it will be appreciated by those ordinarily skilled in the art that other bus systems, such as a bus system using a shared command/address bus, may also be used without departing from the scope of the present invention. It will be further appreciated that the arrangement of the

memory devices 148, and the number of memory devices 148 can be modified without departing from the scope of the present invention.

Figure 2 illustrates a portion of the memory hub 140 according to an embodiment of the present invention. The memory hub 140 includes a local hub circuit 214 coupled to the memory controller/hub interface 134 (Figure 1). The local hub circuit 214 is further coupled to memory devices 148 through the memory bus 150. The local hub circuit 214 includes control logic for processing memory commands issued from the memory controller 128 and for accessing the memory devices 148 over the memory bus 150 to provide the corresponding data when the memory command is directed to the respective memory module 130. The design and operation of such control logic is well known by those ordinarily skilled in the art, and consequently, a more detailed description has been omitted from herein in the interest of brevity. The memory hub 140 further includes a data bypass circuit 286 coupled to the local hub circuit 214. As will be explained in more detail below, the data bypass circuit 286 is used to temporarily capture data passing to a distant memory hub, which allows data returning from another distant memory hub to pass through the memory hub 140 before the captured data continues onto the distant memory hub. Thus, the data bypass circuit 286 provides a data bypass mechanism that can be used to avoid data collisions on the bi-directional memory controller/hub interface 134 to which the memory hub 140 is coupled.

As previously discussed, one approach taken by conventional memory sub-systems to avoid data collision is to delay the execution of one memory command until the completion of another memory command. For example, in typical memory systems a write command issued after a read command would not have been allowed to start until near the completion of the read command in order to avoid the read (i.e., inbound) data colliding with the write (i.e., outbound) data on the memory controller/hub interface 134. In contrast, by employing the memory hub 140 having the data bypass circuit 286, write commands issued after a read command can be sequenced earlier than compared with

conventional memory systems, and consequently, memory commands scheduled after the earlier scheduled write command can be executed sooner as well. .

Figure 3 illustrates a data bypass circuit 300 according to an embodiment of the present invention. The data bypass circuit 300 can be substituted for the data bypass circuit 286 (Figure 2) and can be implemented using conventional designs and circuits well known to those ordinarily skilled in the art. The data bypass circuit 300 includes an input buffer 302 that receives input write data WR-DATA_IN and provides the same to a bypass register/FIFO 304 and a first input of a multiplexer 306. An output of the bypass register/FIFO 304 is coupled to a second input of the multiplexer 306. Selection of which of the two inputs to couple to the output of the multiplexer 306 is made by an enable signal EN generated by a bypass select logic 308. The EN signal is also provided to an input/output buffer 310 as an output enable signal activating or deactivating the input/output buffer 310. The bypass select logic 308 generates the appropriate EN signal in response to an activation signal BYPASS_EN provided by the memory hub controller 128 (Figure 1). Alternatively, the BYPASS_EN signal may be provided from other memory hubs (not shown) that are part of the same memory system. The circuitry of the data bypass circuit is conventional, and it will be appreciated that the circuits of the data bypass circuit 300 can be implemented using conventional designs and circuitry well known in the art.

In operation, WR_DATA_IN received by the data bypass circuit 300 is driven through the input buffer 302 and is provided to the first input of the multiplexer 306. The WR_DATA_IN is also saved in the bypass register/FIFO 304. In response to an inactive BYPASS_EN signal, an active EN signal is generated by the bypass select logic 308. The active EN signal enables output by the input/output buffer 310 and couples the output of the input buffer 302 to the input of the input/output buffer 310 through the multiplexer 306. As a result, the WR_DATA_IN is provided directly to the input of the input/output buffer 310 and the WR_DATA_IN is provided through the data bypass circuit 300 without any bypass. However, in response to an active BYPASS_EN signal, the bypass select logic 308 generates an inactive EN signal, disabling the output function of the

input/output buffer 310 and placing its output in a high-impedance state. Additionally, the inactive EN signal couples the input of the input/output buffer 310 to the output of the bypass register/FIFO 304. In this manner, the WR_DATA_IN is received by the data bypass circuit 300, stored by the bypass register/FIFO 306, and applied to the input of the input/output buffer 310. However, due to the inactive state of the EN signal, the WR_DATA_IN is not provided as output data WR_DATA_OUT by the input/output buffer 310. As a result, the WR_DATA_IN is held in a bypass state until the BYPASS_EN signal becomes inactive, at which time, the EN signal become active again, enabling the input/output buffer 310 to provide the WR_DATA_IN as WR_DATA_OUT data. The multiplexer 306 is also switched back to coupling the output of the input buffer 302 directly to the input of the input/output buffer 310 to allow WR_DATA_IN to pass through the data bypass circuit unhindered.

Operation of the data bypass circuit 286 will be described with reference to Figure 4. Figure 4 is similar to Figure 1, except that Figure 4 has been simplified. In particular, many of the functional blocks of Figure 1 have been omitted, with only the memory modules 130a-130c being shown, and represented by memory hubs 140a-140c. Only one memory device 148a-148c is shown to be coupled to a respective memory hub 140a-140c through a respective memory bus 150a-150c. As with Figure 1, the memory hubs 140a-140c are coupled by a high-speed bi-directional memory controller/hub interface 134 to a memory hub controller 128.

In Figure 4, it is assumed that the memory hub controller 128 has just issued read and write commands, with the read command sequenced prior to the write command. The read command is directed to the memory module 130b and the write command is directed to the memory module 130c. That is, the memory module to which data will be written is further downstream than the memory module from which data is read. In response to the read command, the memory hub 140b begins retrieving the read data (RD) from the memory device 148b, as indicated in Figure 4 by the "(1)". With the read command issued, the write command is then initiated, and the write data (WD) is provided

onto the memory controller/hub interface 134. However, since the memory hub controller 128 is expecting the RD to be returned from the memory module 130b, the memory hub 140a is directed to capture the WD in its data bypass circuit 286a. As a result, the memory hub 286a captures the WD to clear the memory controller/hub interface 134, as indicated in Figure 4 by the "(2)", for the RD to be returned to the memory hub controller 128. When the memory hub 140b has retrieved the RD from the memory device 148b, the RD is then provided to the memory hub controller 128 through the memory controller/hub interface 134, as indicated in Figure 4 by the "(3)" to complete the read request. Upon the RD passing through the memory hub 140a on its way to the memory hub controller 128, the memory hub 140a releases the WD from the data bypass circuit 286a to continue its way to the memory hub 140c. The WD is provided to the memory hub 140c through the high-speed link, which is now clear between the memory hub 140a and 140c. Upon reaching the memory hub 140c, the WD is written in the memory device 148c, as shown in Figure 4 by the "(4)". In an embodiment of the present invention, coordination of the data flow of the RD and WD on the memory controller/hub interface 134 and through the data bypass circuits 286 is under the control of the memory hub controller 128. For example, in the previous example the memory hub controller ensures that any WD flowing in the opposite direction of the RD is out of the way when retrieving RD from the memory module 130b. It will be appreciated, however, that in alternative embodiments data flow through the memory controller/hub interface 134 and the data bypass circuits 286 can be managed differently, such as the memory hub controller 128 sharing coordination of the data flow with the memory hubs 140.

In the previous example, the RD is returned to the memory hub controller 128 as in a conventional memory system. That is, the RD transmitted by the memory devices 148 is provided to the memory controller without any significant delay. However, by employing the previously described data bypass mechanism, write commands can be scheduled earlier than with conventional memory systems. A write command issued after a read command would not have been allowed to start until near the completion of the read

command in typical memory systems. In contrast, embodiments of the present invention allow a subsequently issued write command to be scheduled earlier, thus, reducing the time gap between read and write commands. As a result, commands scheduled behind an earlier scheduled write command have an overall reduced latency.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

1. A memory hub for a hub-based memory module, comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

2. The memory hub of claim 1 wherein the write bypass circuit comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

3. The memory hub of claim 2 wherein the write bypass circuit further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

4. The memory hub of claim 1, further comprising a memory device interface coupled to the data path, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

5. A memory hub for a hub-based memory module, comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

6. The memory hub of claim 5 wherein the data bypass circuit comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

7. The memory hub of claim 6 wherein the data bypass circuit further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

8. The memory hub of claim 5, further comprising a memory device interface coupled to the switching circuit, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

9. The memory hub of claim 8 wherein the memory device interface comprises:

a memory controller coupled to the data path through a memory controller bus and further having a memory device terminal to which a memory device can be coupled;

a write buffer coupled to the memory controller for storing memory requests; and

a cache coupled to the memory controller for storing data.

10. The memory hub of claim 5 wherein the first set of data represents write data and the second set of data represents read data.

11. A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, the memory hub comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

12. The memory module of claim 11 wherein the write bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

13. The memory module of claim 12 wherein the write bypass circuit of the memory hub further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

14. The memory module of claim 11 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

15. The memory module of claim 14 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

16. A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to at least one of the plurality of memory devices, the memory hub comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

17. The memory module of claim 16 wherein the data bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer

input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

18. The memory module of claim 17 wherein the data bypass circuit of the memory hub further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

19. The memory module of claim 16 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

20. The memory module of claim 16 wherein the first set of data represents write data and the second set of data represents read data.

21. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, the memory hub comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

22. The processor-based system of claim 21 wherein the write bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

23. The processor-based system of claim 22 wherein the write bypass circuit of the memory hub further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

24. The processor-based system of claim 21 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

25. The processor-based system of claim 24 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

26. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to at least one of the plurality of memory devices, the memory hub comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

27. The processor-based system of claim 26 wherein the data bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

28. The processor-based system of claim 27 wherein the data bypass circuit of the memory hub further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

29. The processor-based system of claim 26 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

30. The processor-based system of claim 29 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

31. The processor-based system of claim 26 wherein the first set of data represents write data and the second set of data represents read data.

32. A method for writing data to a memory location in a memory system coupled to a memory bus, comprising:

accessing read data in the memory system;

providing write data to the memory system on the memory bus;

coupling the write data to a register in the memory system for temporary storage of the write data;

coupling the read data to the memory bus and providing the read data for reading;

coupling the write data stored in the register to the memory bus; and

writing the write data to the memory location.

33. The method of claim 32, further comprising issuing a read command to the memory system prior to issuing a write command to the memory system.

34. The method of claim 32 wherein providing the write data to the memory system comprises providing the write data through at least one memory module of the memory system prior to coupling the write data to the register.

35. The method of claim 32 wherein the memory system includes a plurality of memory modules coupled in series on the memory bus, and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed.

36. A method for executing memory commands in a memory system having a memory bus, the method comprising:

issuing a read command to the memory system;

issuing a write command to a memory location in the memory system and providing write data to the memory bus of the memory system;

accessing read data in the memory system;

in the memory system, decoupling the write data from the memory bus;

receiving the read data on the memory bus from the memory system;

recoupling the write data to the memory bus; and

resuming the write command to the memory location.

37. The method of claim 36 wherein issuing the read command to the memory system precedes issuing the write command to the memory system.

38. The method of claim 36, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

39. The method of claim 36 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

40. A method for executing read and write commands in a memory system having a memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system

retrieving read data from the first memory location;

providing write data to the memory bus of the memory system;

in the memory system, bypassing the read data on the memory bus;

receiving the read data on the memory bus from the memory system; and

providing the write data to the memory bus.

41. The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM

ABSTRACT OF THE DISCLOSURE

A memory hub includes first and second link interfaces for coupling to respective data busses, a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces, and further includes a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored. A method for writing data to a memory location in a memory system is provided which includes accessing read data in the memory system, providing write data to the memory system, and coupling the write data to a register for temporary storage. The write data is recoupled to the memory bus and written to the memory location following provision of the read data.

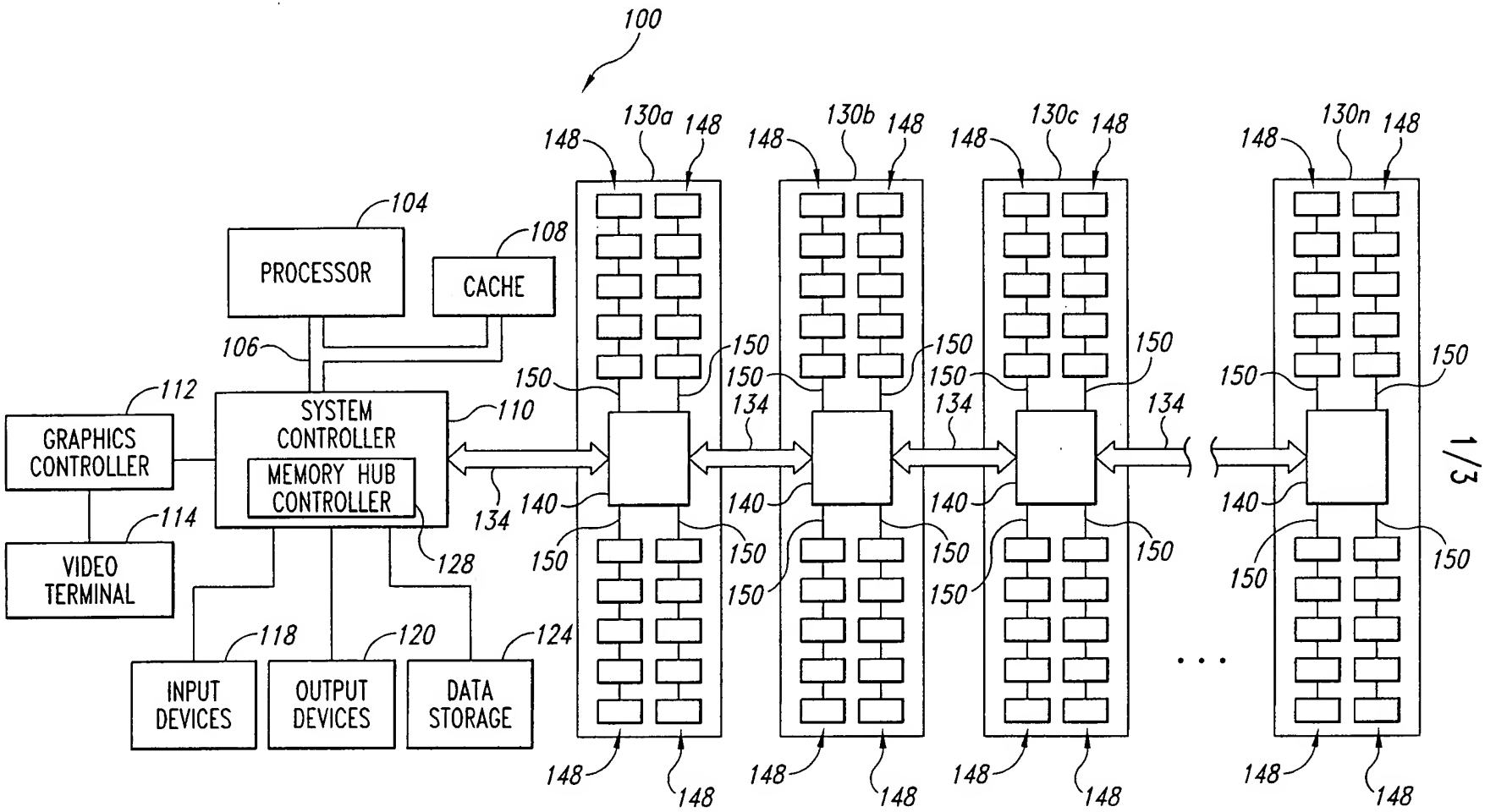
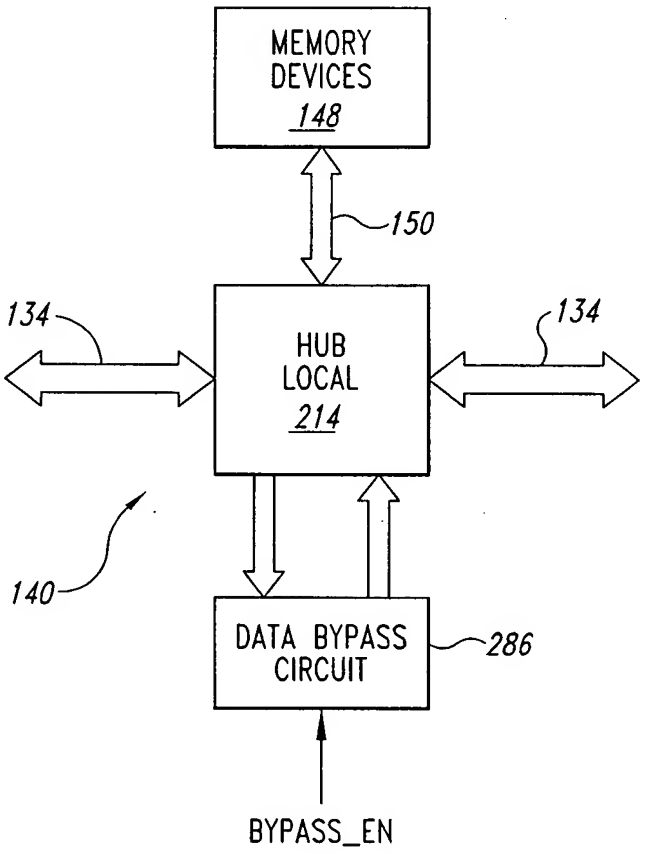

100
PROCESSOR
104
CACHE
108
106
GRAPHICS CONTROLLER
112
SYSTEM CONTROLLER
110
MEMORY HUB CONTROLLER
128
VIDEO TERMINAL
114
INPUT DEVICES
118
OUTPUT DEVICES
120
DATA STORAGE
124
130a
130b
130c
130n
148
150
134
140

Fig. 1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DEVICES
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150
134
134
HUB
LOCAL
214
140
DATA BYPASS
CIRCUIT
286
BYPASS_EN

Fig. 2

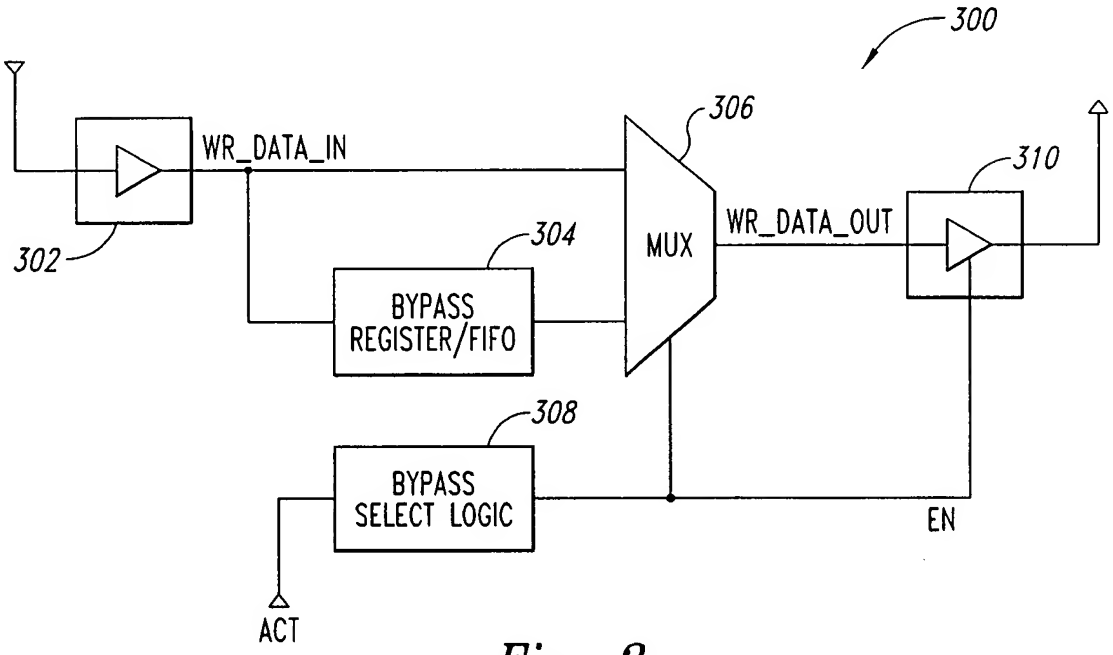

300
306
WR_DATA_IN
310
WR_DATA_OUT
MUX
302
304
BYPASS
REGISTER/FIFO
308
BYPASS
SELECT LOGIC
EN
ACT

Fig. 3

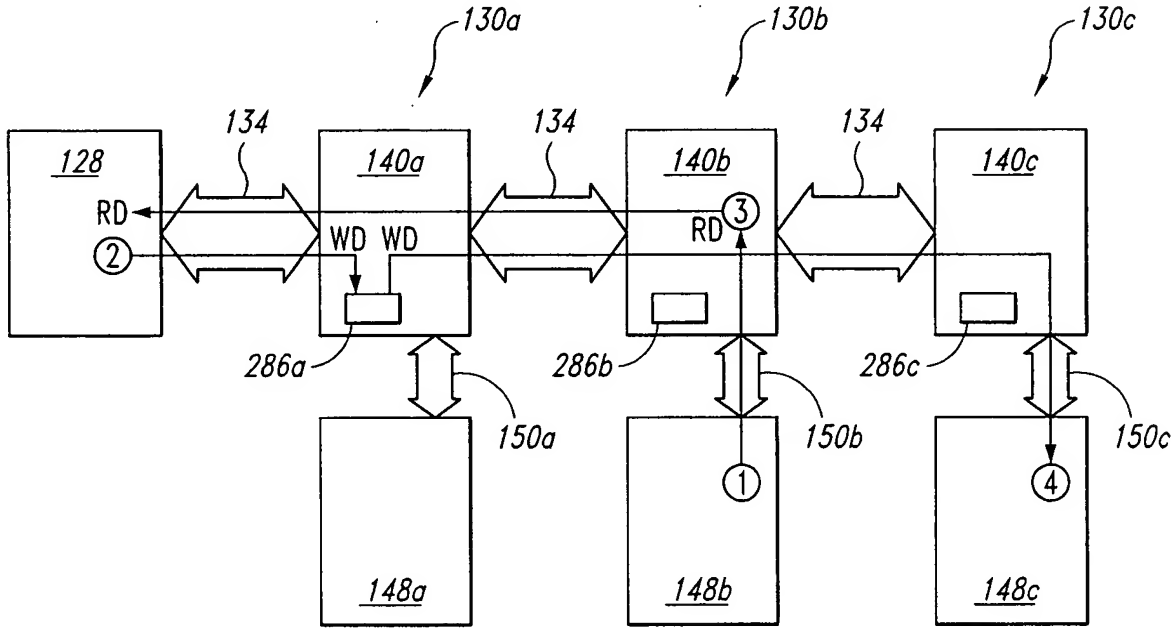

130a
130b
130c
134
134
134
128
140a
140b
140c
RD
2
WD WD
RD
3
286a
286b
286c
150a
150b
150c
1
4
148a
148b
148c

Fig. 4

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450. Alexandria, VA 22313-1450.

June 5, 2007
Date

Sherri A. Phillips

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/773,583	Confirmation No.	: 6732
Applicants	: Douglas A. Larson and Jeffrey J. Cronin		
Filed	: February 5, 2004	Attorney Docket No.	: 501296.01 (30266/US)
Art Unit	: 2188	Customer No.	: 27,076
Examiner	: Duc T. Doan		
Title	: APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM		

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF (37 C.F.R. § 41.37)

Sir:

This brief is in furtherance of the Notice of Appeal filed in this case on April 5, 2007. The fees required under Section 41.20, and any required request for extension of time for filing this brief and fees therefore, are dealt with in the accompanying transmittal letter.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee of this application, Micron Technology, Inc., a Delaware Corporation having a principal place of business in Boise, Idaho.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to appellants, the Appellants' legal representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-43.

B. STATUS OF ALL THE CLAIMS

1. Claims canceled: 1-39.
2. Claims withdrawn from consideration but not canceled: None.
3. Claims objected to: None.
4. Claims allowed or confirmed: None.
5. Claims rejected: 36-43.

C. CLAIMS ON APPEAL

The claims on appeal are: 40-43.

IV. STATUS OF AMENDMENTS

Appellants canceled claims 1-4, 11-15, 21-25, and 32-39 after final rejection. (Response dated February 5, 2007 attached hereto as Exhibit B and the Supplemental Response dated June 5, 2007 attached hereto as Exhibit C).

V. SUMMARY OF CLAIMED SUBJECT MATTER

1. Introduction

The present application is directed toward solving the problem of data collisions on a bi-directional data bus in a memory system. In one embodiment shown in Figure 1, a memory system has multiple memory modules 130a-n connected to each other in series and to a memory hub controller 128 via a bi-directional data bus. Data collisions can occur on a bi-directional data bus when a read command is issued before a write command. For example, as read data is heading downstream from a memory device on memory module 130c and write data is simultaneously heading upstream from the memory hub controller 128 to memory module 130n, the read data and the write data would collide. The present application prevents this data collision by using a bypass circuit 286. In one embodiment, the bypass circuit 286 is capable of temporarily storing data passing through a respective memory hub 140. As in the example provided above, as the read data is about to head downstream toward memory module 130b from memory module 130c, the write data is heading upstream from memory module 130a toward memory module 130b. In order to prevent a data collision, the write data is temporarily stored in the bypass circuit 286 in the memory hub 140 of memory module 130b. While the write data is stored in the bypass circuit 286, the read data continues downstream to memory module 130a. Once the read data passes through memory module 130b on its way to memory module 130a, the write data may be recoupled to the bi-directional data bus to continue its way upstream to memory module 130n. Therefore, when a read command is issued before a write command, the corresponding write data can be sent upstream before the read latency of the previously issued read command is complete. *Specification,*. at page 8, lines 12-27, page 10, lines 21-28, page 11, lines 1-22 and Figure 3. (Specification attached hereto as Exhibit D).

2. Claim 40

Claim 40 is directed toward a method for executing read and write commands in a memory system having a bidirectional memory bus. *Specification,* at page 5, lines 15-17. The method of claim 40 includes "issuing a read command to access a first memory location in the memory system" and "before completion of the read command, scheduling a write command to

write data to a second memory location in the memory system." In one embodiment, a read command is issued by the memory hub controller 128 to access a first memory location in a memory system. Before completing the read command, a write command is scheduled by the memory hub controller 128 to write data to a second memory location in the memory system. *Id.* at page 10, lines 21-28.

In addition, claim 40 includes "retrieving read data from the first memory location." In one embodiment, the read data is retrieved from the first memory location. *Id.* at page 10, lines 21-28.

Claim 40 further includes "prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system." In one embodiment, prior to the memory hub controller 128 receiving the read data on the memory bus, the write data corresponding to the write command is provided to the bidirectional memory bus. *Id.* at page 10, lines 27-28 and page 11, line 1.

Claim 40 further includes "in the memory system, bypassing the read data on the bidirectional memory bus." In one embodiment, the read data on the bidirectional memory bus is bypassed while in the memory system when a bypass circuit 286 captures the write data so that read data can be sent to the memory hub controller 128. *Id.* at page 11, lines 1-14. Finally, claim 40 includes "receiving the read data on the bidirectional memory bus from the memory system" and "providing the write data to the bidirectional memory bus." In one embodiment, the read data on the bidirectional memory bus is received by the memory hub controller 128 from the memory system. *Id.* In addition, the write data is provided back to the bidirectional memory bus. *Id.*

VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL

The only ground of rejection to be reviewed on appeal is whether claim 40, as well as any claims dependent thereon, are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent Application No. 2005/0105350 to Zimmerman ("Zimmerman"), in view of U.S. Patent No. 6,622,188 to Goodwin et al. ("Goodwin") and further in view of U.S. Patent No. 6,901,494 to Zumkehr et al. ("Zumkehr "). (Office Action dated December 5, 2006 attached hereto as Exhibit A).

VII. ARGUMENTS

I. Claim 40 are Patentable over Zimmerman in view of Goodwin and further in view of Zumkehr

A. The Subject Matter of Claims 40

Claim 40 reads as follows:

> 40. A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:
>
> issuing a read command to access a first memory location in the memory system;
>
> before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;
>
> retrieving read data from the first memory location;
>
> prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;
>
> in the memory system, bypassing the read data on the bidirectional memory bus;
>
> receiving the read data on the bidirectional memory bus from the memory system; and
>
> providing the write data to the bidirectional memory bus.

B. The Subject Matter Disclosed in the Zimmerman Reference

The Zimmerman reference is directed to a memory test mechanism for buffered-memory-module memory subsystems. The Zimmerman reference provides a testing method for evaluating individual memory modules and individual module-to-module memory channels independent of the host and host memory channel. The Zimmerman reference is cited by the

Examiner for disclosing a memory system that includes multiple hub-based memory modules with data paths that interlink the memory module hubs. Although the Zimmerman reference does disclose the memory system described above, it and no other reference cited by the Examiner discloses data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write data.

C. The Subject Matter Disclosed in the Goodwin Reference

The Goodwin reference is directed to an I^2C bus expansion apparatus that permits multiple bus devices of the same group to reside on an I^2C bus in a data processing system. The I^2C bus is a 2-wire bidirectional serial bus for communication between bus devices in a data processing system. The Goodwin reference is cited by the Examiner for disclosing a bidirectional data bus. Although the Goodwin reference discloses a bidirectional data bus, it and no other reference cited by the Examiner discloses data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write data.

D. The Subject Matter Disclosed in the Zumkehr Reference

The Zumkehr reference discloses a RAMBUS control and data bus connecting a RAMBUS memory controller 210 to a translator hub 220, and a SDRAM control and data bus connecting the translator hub 220 to SDRAM memory devices 161. *Zumkehr Specification*, Figure 2. SDRAM devices require write data to be sent with write commands. Therefore in prior systems, write commands were delayed until the write data could be sent from the RAMBUS memory controller to the SDRAM device via the translator hub. Therefore, both the write command and corresponding write data could not be sent until after the read latency of the previous read command was met. The Zumkehr reference, however, teaches the ability to issue a write command without sending the corresponding write data by storing the write command in a write buffer within the translator hub. By being able to send a write command without corresponding write data, the Zumkehr reference teaches the ability to issue a write command after a read command has been issued; however, the Zumkehr reference does not teach

the ability to issue the corresponding write data before the completion of the latency of the previous issued read command. *Zumkehr Specification*, column 4, lines 45-68 – column 5, lines 1-13.

In Figure 5A, the Zumkehr reference discloses a timing diagram of a memory system where the translator hub does not include a write buffer and Figure 5B shows a timing diagram where the translator hub does include a write buffer. In Figure 5A, a write command following a read command is delayed by a period corresponding to the read latency of the previous read command. In contrast, Figure 5B, which includes a write buffer in the translator hub, shows that a new write command 520B following a read command 501B can be issued before the read latency of the previously issued read command 501B is met. Once the new write command 520B is received in the translator hub, *a previous* write command 522B and corresponding write data 525B already stored in the translator hub are sent to the memory devices. However, the write data 527B associated with the new write command 520B remains in the memory controller and cannot be issued until *after* the read latency of the previously issued read command 501B is met. *Zumkehr Specification*, column 5, lines 39-44, column 6, lines 53-67 – column 7, lines 1-49 and Figures 5A and 5B. Therefore, the Zumkehr reference does not disclose or fairly suggest data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write.

E. Summary of the Rejection

The final rejection dated December 5, 2006 rejects claim 40 as being unpatentable under 35 U.S.C. § 103(a) over Zimmerman, in view of Goodwin, and further in view of Zumkehr.

In the Office Action, the Examiner rejected claim 40 under the same rationale as cancelled claim 1. *Office Action*, page 5, line 7 and page 7, lines 8-13, respectively. Under claim 1, the Examiner contends that Zumkehr discloses a write bypass circuit coupled to a direct data path and temporarily storing write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred

through the direct data path. In particular, the Examiner contends that the multiplexer or the write buffer in Figure 6 of the Zumkehr reference is analogous to the write bypass circuit of claim 1.

Claim 40 is patentably distinct from claim 1. Cancelled claim 1 disclosed a write bypass circuit coupled to a bidirectional data path capable of temporarily storing write data to allow read data to pass through the bidirectional data path and then recoupling the stored write data to the data path. Therefore, write data and read data could be on the bidirectional data path at the same time, moving in opposite directions and still avoid a data collision. Claim 1 did not require that the write command and corresponding write data be issued before completion of the read command. However, method claim 40 requires scheduling a write command to write data before completion of a previously issued read command.

It appears that the Examiner contends that the Zumkehr reference discloses a method of bypassing write data regardless of whether the latency of a previous read command is met. The Appellants contend that the Zumkehr reference does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued followed by a write command and corresponding write data, when the write command and corresponding write data are issued before the read latency is met.

F. The Zimmerman, Goodman, and Zumkehr References, in Combination or by Themselves, Do Not Disclose All of the Limitations of Claim 40

The Zumkehr reference was cited by the Examiner for disclosing a method of bypassing the read data on the bidirectional memory bus of claim 40. The Examiner contends that the multiplexer 650 or the write buffers 330 within the translator hub 220 have the capability of storing write data in order to prevent data collisions on a bidirectional data bus similar to the bypass circuit of the present application. The Zumkehr reference, however, does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued, and before the read latency is met, issuing a write command and corresponding write.

As described above, the Zumkehr reference discloses a bus connecting a RAMBUS memory controller 210 to a translator hub 220, and an SDRAM bus connecting the translator hub 220 to SDRAM memory devices 161. The write buffer in the translator hub is capable of receiving a write command at a different time than the corresponding write data and sending the write command and corresponding write data to the SDRAM devices. *Id.* at column 5, lines 39-44 and Figure 5B. This improves the performance of the data transfer, because the write command can be issued from the memory controller without requiring the corresponding write data to be sent from the memory controller one clock cycle later. For example, a situation in which the corresponding write data can not be sent with the write command exits when a read command has already been issued. The write data must wait for the read latency of the previously issued read command to be met before it can be transferred to the translator hub. *Id.* at column 7, lines 18-20 stating "the RAMBUS memory controller 210 defers write data transfer on a write command until the read latency of a previous read command is met". Once the translator hub receives the new write command, *a previously issued* write command and corresponding write data that were stored in the translator hub *before* the read command was issued may be sent to the memory devices before the read latency of the read command is complete. *See, Id.* at column 6, lines 53-67 – column 7, lines 1-49, and Figure 5B. Therefore, only the write data that was already issued and located on the translator hub may go onto the data bus after a subsequent read command is issued. If write data were issued from the memory hub after a read command was issued, there would be a collision on the RAMBUS data bus as the read data is heading downstream to the memory controller and the write data is heading upstream to the translator hub. Therefore, the Zumkehr reference does not disclose or fairly suggest the capability of preventing a data collision on a bidirectional data bus when a read command is issued, but before the read latency is met, issuing a write command *and corresponding write data*.. Neither the Zimmerman reference nor the Goodman reference make up for the deficiencies of the Zumkehr reference.

Turning now to the claims, the Zimmerman, Goodman, and Zumkehr references, in combination or alone, do not disclose all the limitations of claim 40. A claim

rejected under 35 U.S.C. § 103(a) must teach or suggest all of the claim limitations. M.P.E.P. 706.02(j).

Method claim 40 requires, in part, issuing a read command, *before completion of the read command*, scheduling a write command, retrieving the read data, but prior to receiving the read data from the memory system, providing write data corresponding to the write command to the bidirectional memory bus, and in the memory system, bypassing the read data on the bidirectional memory bus. As alluded to above, the Zumkehr reference fails to disclose or suggest the above limitation. Rather, the Zumkehr reference waits for the read latency of a read command to end before issuing the write data that corresponds to a write command issued after the read command. In contrast, method claim 40 requires providing write data to the bidirectional memory bus prior to receiving the read data from the memory system. Therefore, claim 40 is allowable over the Zumkehr reference.

Neither the Zimmerman reference nor the Goodwin reference make up for the deficiencies in the Zumkehr reference discussed above. In fact, the Examiner explicitly admits in the Final Office Action dated December 5, 2006 that neither the Zimmerman reference nor the Goodwin reference disclose a bypath data path. *Office Action*, page 4, line 6.

For all of the reasons explained above, neither the Zumkehr reference, the Zimmerman reference, nor the Goodwin reference, in combination or by themselves, disclose or fairly suggest all elements of claim 40 in the present application. Therefore, the rejection of claim 40, as well as claims dependent thereon, should be reversed.

VIII. CLAIMS APPENDIX

The text of the claims involved in the appeal are:

40. A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

IX. EVIDENCE APPENDIX

1. Office Action dated December 5, 2006 and prior art cited therein attached hereto as Exhibit A.

2. Response dated February 5, 2007 attached hereto as Exhibit B.

3. Supplemental Response dated June 5, 2007 attached hereto as Exhibit C.

4. Applicants' Specification, filed February 5, 2004 attached hereto as Exhibit D.

X. RELATED PROCEEDINGS APPENDIX

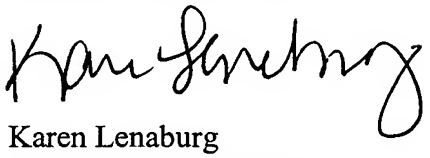
None.

XI. CONCLUSION

For all of the reasons stated above, the rejection of claims 40-43 should be reversed.

Respectfully submitted,

DORSEY & WHITNEY LLP



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,583	02/05/2004	Douglas A. Larson	501296.01 (30266/US)	6732

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

FINAL REJECTION

2 mo. Response Due: February 5, 2007
3 mo. Response Due: March 5, 2007
Notice of Appeal Due: June 5, 2007
(6 mo. period ends/3 mo. ext. of time required - will go abandoned)

AJS

Office Action Summary	Application No. 10/773,583	Applicant(s) LARSON ET AL.	
	Examiner Duc T. Doan	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,11-15,21-25 and 32-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,11-15,21-25 and 32-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 6/19/2006
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-43 have been presented for examination in this application. In response to the last office action, claims 1-3,11-13,21-23,32,36,40 have been amended, claims 5-10,16-20,26-31 have been canceled. As the result, claims 1-4,11-15,21-25,32-43 are pending in this application.

Claims 1-4,11-15,21-25,32-43 are rejected.

All rejections and objections not explicitly repeated below are withdrawn.

Applicant's amendments/remarks filed 9/19/06 have been fully considered but they are mooted in view of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

The information disclosure statements filed 9/19/06 fails to comply with the provisions of 37 CFR 1.97, 1.98 because it does not list any prior art to be considered. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,4,11,14-15,21,24-25,32-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350), in view of Goodwin et al (US 6622188), and further in view of Zumkehr (US 6901494).

As in claim 1, Zimmerman describes a memory hub for a hub-based memory module (Zimmerman's Fig 2: MMB, paragraph 17), comprising: first and second link interfaces for coupling to respective data busses; a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces (Zimmerman's Fig 2, links 112 on both sides of MMB; paragraphs 15);

Zimmerman does not disclose the claim's aspect of a bidirectional data bus operable to transfer both read and write data. However, Goodwin discloses a mechanism in which multiple memory devices are connected to a bidirectional bus as depicts in Goodwin's Fig 2: Expansion devices. It would have been obvious to one of ordinary skill in the art at the time of invention to include bi directional bus mechanism as suggested by Goodwin in Zimmerman's system thereby further allow read and write data in expansion devices such as memory devices to be transferred effectively over the same bidirectional data bus (Goodwin's column 1 lines 10-35). Zimmerman

discloses first and second link interfaces for coupling to respective portions of the bus the portion of the data bus (i.e Host side and downstream sides of the links 132, 142, each segment represent a portion of the data bus). Goodwin further discloses the expansion memory #216 having the direct data path (SCL 236 through which data is transferred between the first (i.e link to expansion memory 215) and second link (i.e link to expansion memory 218) interfaces, Zimmerman and Goodwin do not expressly disclose the claim's detail of bypath data path. However, Zumkehr's discloses a bypath data path having a write bypass circuit coupled to the direct data path and temporarily store the write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred through the direct data path (Zumkehr's Fig 7 #730 discloses the circuits in the translator hub providing a direct data path, in which the write data received by the translator hub (Fig 2: #220) is immediately and directly forwarding to the downstream device; Zumkehr's Fig 6 discloses a multiplexer (i.e write by pass circuit) that allowing temporary stored the write data while allowing the read data to be transferred through the direct data path, directly to the upstream device; subsequently the multiplexer recouple the stored write data and sending to the downstream device; Zumkehr's column 7 lines 17-23 discloses the write command received by the translator circuit must be delayed and allowing the read command to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory controller hub circuits and methods as suggested by Zumkehr in Zimmerman's system to allow transferring read data while

temporary storing write data, thereby resulting in more efficiently usage of the memory bus in the system (Zumkehr's column 6 lines 35-60; read and write data transferring through the same bidirectional data bus Fig 3: #350 data signals).

As in claim 4, Zimmerman's Fig 5 describes a memory device interface coupled to the data path, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

Claims 11,21,32,36 rejected based on the same rationale as in the rejection of claim 1.

Claims 14,24 rejected based on the same rationale as in the rejection of claim 4.

As in claim 15, Zimmerman discloses a memory controller (Fig 2: MMB) coupled to a data path through a memory controller bus (Zimmerman's Fig 2: 112); and further coupled to at least one of the plurality of memory devices through a memory device bus (MMB couples to memory device DRAM obviously vie DRAM memory device bus), a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device (Zimmerman's paragraph 15 discloses the buffered memory modules/controller logic to store the memory requests and to store the memory data receiving from the host).

Claim 21 rejected based on the same rationale as in the rejection of claim 1.Zimmerman's Fig 1 further discloses a processor (Zimmerman's Fig 1: #20) and processor bus connecting the processor to the system controller (Zimmerman's Fig 1: #30 MCH), which obviously having associating ports connecting to peripheral devices such as memory data storage devices

(Zimmerman's Fig 2: DRAM); a memory module (Zimmerman's Fig 3a) comprising memory hub (Fig 2: MMB). The remaining limitation of claim 21 is rejected based on the same rationale as of claim 1.

Claim 25 rejected based on the same rationale as of claim 15.

As in claim 33, Zumkehr's column 7 lines 17-23 discloses the write command received by the translator circuit must be delayed and allowing the read command to be issued earlier and, to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals.

As in claim 34, Zumkehr describes translator circuit to translate a write command to an sdram write command for the memory device, in addition to the FIFO queue for other write commands being received (Zumkehr's column 5 lines 5-12).

As in claim 35, Zimmerman discloses wherein the memory system includes a plurality of memory modules coupled in series on the memory bus (Zimmerman's Fig 2 DRAM memory modules #120, #130 in serial on the memory bus), and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed (Zimmrman's Fig 2 discloses writing to memory module #130 located downstream from memory module #120 in which the read data is accessed by the host #110).

Claim 37 rejected based on the same rationale of claim 33.

As in claim 38, Zumkehr's describes the write buffer to temporary store write data request (zumkerhr's Fig 3: #330).

As in claim 39, the claim recites wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus. Zumkehr further describes the write buffer in MMB is provided to temporary store data from host and thus decoupling the host to handle another accessing data on the memory bus (Zumkehr's Fig 5)

Claim 40 rejected based on the same rationale as of claim 1. Zimmerman further discloses a memory system with multiple buffered memory modules; each memory buffer module can buffer write and read command issued from the host (Fig 2: #110). Thus the host can continue issuing commands to these buffered memory modules in concurrently manner, that is the read command can be issued to memory module Fig 2: #130 before issuing the write command to memory module Fig 2: #120.

As in claim 41, the claim rejected based on the same rationale as of claim 40. Zumkehr's column 7 lines 17-23 further discloses the write command received by the translator circuit must be delayed for a time period and allowing the read command to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals. Therefore the collision on the bi-direction data bus can be averted.

As in claims 42-43, Zumkehr discloses the write data is stored temporary in Fig 3: #330 to avoid the collision with the read data receiving from bi-directional data signal Fig 2: 350's

data signals (claim 42); wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus (claim 43; Zumkehr discloses a FIFO to temporary store write commands (i.e sending the write data of the first write command to at least one memory module, receiving read command, storing the data of the second write command in the FIFO before decoupling and allowing the data of a read travels through the memory bus (from Fig 3: #350 data signals to the host, Fig 3: #310 data signal).

Claims 2-3,12-13,22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350), in view of Goodwin et al (US 6622188), Zumkehr (US 6901494) as applied to claims 1,11,21 respectively, and in view of Garcia et al (US 6782435).

As in claim 2, although Zumkehr's Fig 6: #650 discloses the multiplexer providing the directly data path (read data) and the bypass data path (write data), Zumkehr does not expressly disclose the claim's detail of the multiplexer. However, Garcia's Fig 2 teaches in detail a multiplex circuit comprises a multiplexer, a bypass selection signal, and a register to temporary store write data being received. It would have been obvious to one of ordinary skill in the art at the time of invention to include the temporary storage and the multiplexer circuits as suggested by Garcia in Zimmerman's system to temporary reordering the transmitting data thereby allowing accessing memory device with minimum latency and maximizing the throughput of he overall system (Garcia's column 1, lines 48-62).

As in claims 3, the claim recite wherein the write bypass circuit further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register. The claim rejected based on the same rationale as in the rejection of claim 2.

Claims 12,22 rejected based on the same rationale as of claim 2.

Claims 13,23 rejected based on the same rationale as of claim 3.

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

Regarding remarks on pages 11-12 for the Zimmerman's expressly teaching of the bidirectional data bus. It's mooted in view of the new reference Goodwin et al, new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

Regarding the remark on pages 12-17, Applicant contends that Zumkehr does not provide a direct data path for the write data to be provided to the down stream device (i.e the sdram device). Examiner respectfully disagrees. Zumkehr's Fig 6 discloses a multiplexer in the translator hub that provides a data path directly to the downstream device, when it received the write data sent from the host's Fig 3: #210; receiving at its buffer Zumker's Fig 3: #330 and sending directly to down stream devices Fig 3: #161. Examiner notes that the same mechanism is

disclosed in specification's Fig 3, that is host's data is received at a receiving buffer Fig 3: 302 and subsequently it is sent directly to down stream device.

Applicant contends that Zumkehr's buffering circuits do not provide avoiding the data collision between data heading the opposite directions on the bidirectional data paths. Examiner respectfully disagrees, Zumkehr discloses write buffers that temporary store write data of write requests so that the read data of the read command can be sent on the opposite direction toward the host on the same bidirectional bus, Fig 3: #350 data signals. Thus the write data toward the down stream device is temporary stored, delay and avoids the collision with the read data traveling in opposite direction on the same bidirectional data bus (see Zumkehr's column 6 lines 22-30).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP 706.07(a). Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
11/29/06

FORM PTO-1449 (REV.7-80) | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT

(Use multiple sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.
501296.01 (30266/US)	10/773,583
APPLICANT(S)	
Douglas A. Larson and Jeffrey J. Cronin	
FILING DATE	GROUP ART UNIT
February 5, 2004	2188

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
DD	AA	6,324,485 B1	11/27/01	Ellis	702	117	
	AB	6,526,483 B1	02/25/03	Cho et al.	711	154	
	AC	6,636,912 B2	10/21/03	Ajanovic et al.	710	105	
	AD	2003/0005344 A1	01/02/03	Bhamidipati et al.	713	400	
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	AH	2005/0149603 A1	07/07/05	DeSota et al.	709	200	
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AM							
	AN							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

DD	AO	Rambus, Inc., "Direct Rambus™ Technology Disclosure", October 1997. pp. 1-16.
	AP	
	AQ	

EXAMINER	DATE CONSIDERED
Sue Doan	11/28/06

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

Notice of References Cited	Application/Control No. 10/773,583	Applicant(s)/Patent Under Reexamination LARSON ET AL.	
	Examiner Duc T. Doan	Art Unit 2188	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,622,188	09-2003	Goodwin et al.	710/105
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE - EXAMINING GROUP 2100

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

February 7, 2007 _____
Date Sherri A. Phillips

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/773,583	Confirmation No.	: 6732
Applicants	: Douglas A. Larson and Jeffrey J. Cronin		
Filed	: February 5, 2004	Attorney Docket No.	: 501296.01 (30266/US)
Art Unit	: 2188	Customer No.	: 27,076
Examiner	: Duc T. Doan		
Title	: APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE UNDER 37 C.F.R. § 1.116

Sir:

Applicants acknowledge receipt of the Office Action dated December 5, 2006. Please amend the above-captioned patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks begin on page 7 of this paper.

Amendments to the Specification:

Please replace paragraph [23] with the following amended paragraph:

--In operation, WR_DATA_IN received by the data bypass circuit 300 is driven through the input buffer 302 and is provided to the first input of the multiplexer 306. The WR_DATA_IN is also saved in the bypass register/FIFO 304. In response to an inactive ACT signal, an active EN signal is generated by the bypass select logic 308. The active EN signal enables output by the input/output buffer 310 and couples the output of the input buffer 302 to the input of the input/output buffer 310 through the multiplexer 306. As a result, the WR_DATA_IN is provided directly to the input of the input/output buffer 310 and the WR_DATA_IN is provided through the data bypass circuit 300 without any bypass. However, in response to an active ACT signal, the bypass select logic 308 generates an inactive EN signal, disabling the output function of the input/output buffer 310 and placing its output in a high-impedance state. Additionally, the inactive EN signal couples the input of the input/output buffer 310 to the output of the bypass register/FIFO 304. In this manner, the WR_DATA_IN is received by the data bypass circuit 300, stored by the bypass register/FIFO ~~306~~ 304, and applied to the input of the input/output buffer 310. However, due to the inactive state of the EN signal, the WR_DATA_IN is not provided as output data WR_DATA_OUT by the input/output buffer 310. As a result, the WR_DATA_IN is held in a bypass state until the ACT signal becomes inactive, at which time, the EN signal become active again, enabling the input/output buffer 310 to provide the WR_DATA_IN as WR_DATA_OUT data. The multiplexer 306 is also switched back to coupling the output of the input buffer 302 directly to the input of the input/output buffer 310 to allow WR_DATA_IN to pass through the data bypass circuit unhindered.--

Please replace paragraph [25] with the following amended paragraph:

--In Figure 4, it is assumed that the memory hub controller 128 has just issued read and write commands, with the read command sequenced prior to the write command. The read command is directed to the memory module 130b and the write command is directed to the memory module 130c. That is, the memory module to which data will be written is further downstream than the memory module from which data is read. In response to the read command, the memory hub 140b begins retrieving the read data (RD) from the memory device 148b, as indicated in Figure 4 by the "(1)". With the read command issued, the write command

is then initiated, and the write data (WD) is provided onto the high-speed link 134. However, since the memory hub controller 128 is expecting the RD to be returned from the memory module 130b, the memory hub 140a is directed to capture the WD in its data bypass circuit 286a. As a result, the ~~memory hub~~ data bypass circuit 286a captures the WD to clear the high-speed link 134, as indicated in Figure 4 by the "(2)", for the RD to be returned to the memory hub controller 128. When the memory hub 140b has retrieved the RD from the memory device 148b, and has indication from the memory hub 140a that the WD has been successfully captured by the data bypass circuit 286a, the RD is then provided to the memory hub controller 128 through the high-speed link 134, as indicated in Figure 4 by the "(3)" to complete the read request. Upon the RD passing through the memory hub 140a on its way to the memory hub controller 128, the memory hub 140a releases the WD from the data bypass circuit 286a to continue its way to the memory hub 140c. The WD is provided to the memory hub 140c through the high-speed link, which is now clear between the memory hub 140a and 140c. Upon reaching the memory hub 140c, the WD is written in the memory device 148c, as shown in Figure 4 by the "(4)".--

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 1-4, 11-15 and 21-25, and amend claims 32 and 40 as follows:

Listing of Claims:

1-31. (Canceled)

32. (Currently Amended) A method for writing data to a memory location in a memory system coupled to a bidirectional memory bus transmitting both read and write data, comprising:

~~accessing read data in~~ issuing a read command to the memory system;

providing a write command and corresponding write data to the memory system on the bidirectional memory bus, after issuing the read command;

coupling the write data to a register in the memory system for temporary storage of the write data to allow the read data to be returned on the bidirectional data bus after the write data is provided to the same and before the write data has been written;

coupling the read data to the bidirectional memory bus and providing the read data for reading;

coupling the write data stored in the register to the bidirectional memory bus; and

writing the write data to the memory location.

33. (Original) The method of claim 32, further comprising issuing a read command to the memory system prior to issuing a write command to the memory system.

34. (Original) The method of claim 32 wherein providing the write data to the memory system comprises providing the write data through at least one memory module of the memory system prior to coupling the write data to the register.

35. (Original) The method of claim 32 wherein the memory system includes a plurality of memory modules coupled in series on the memory bus, and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed.

36. (Previously Presented) A method for executing memory commands in a memory system having a memory bus on which both read and write data can be coupled, the method comprising:

issuing a read command to the memory system;

issuing a write command to a memory location in the memory system and providing write data for the write command to the memory bus of the memory system after issuing the read command;

accessing read data in the memory system;

in the memory system, decoupling the write data from the memory bus;

receiving the read data on the memory bus from the memory system;

recoupling the write data to the memory bus; and

resuming the write command to the memory location.

37. (Original) The method of claim 36 wherein issuing the read command to the memory system precedes issuing the write command to the memory system.

38. (Original) The method of claim 36, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

39. (Original) The method of claim 36 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

40. (Currently Amended) A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. (Original) The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. (Original) The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. (Original) The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

REMARKS

The specification has been amended in order to resolve obvious errors. No new matter was added.

The Applicants would like to thank the Examiner for the telephone interview conducted on February 1, 2007. During the interview the Applicants stated that the write buffer in the Zumkehr patent, Patent No. 6,901,494, does not disclose a bypass data path having a write bypass circuit coupled to a direct data pass operable to temporarily store the write data to allow read data to be transferred through the direct data path. The Examiner did not agree. The Examiner suggested that the Applicants draft an argument for his Supervisor to review. The Applicants would like to thank the Examiner and his Supervisor for the opportunity to have the argument reviewed by the Examiner's Supervisor.

After the interview, Applicants' attorney spent a great deal of time studying the Zumkehr patent and now has a better understanding of the Examiner's position. Applicants admit that there are some similarities between subject matter disclosed in the present application and the Zumkehr patent for situations in which the write data is passed from the controller 210 to the translator hub 220 *before* a read command is applied to the hub 220. For example in Zumkehr, write data is passed from the controller 210 to the translator hub 220 before a read command is passed from the controller 210 to the translator hub 220 and from the translator hub 220 to the appropriate memory device 161. The read data is then passed from the memory device 161 to the translator hub 220. A write command corresponding to the previous write data is then sent from the controller 210 to the translator hub 220. During the time the read data is being sent from the translator hub 220 to the controller 210, the write data also is sent from the translator hub 220 to the appropriate memory device 161. Therefore, data is being transferred on the bus at the same time. *Zumkehr Specification*, Figure 5B and column 6, lines 53-67 - column 7, lines 1-49.

On the other hand, there are differences that are significant for situations where, as in applicants' system, the write command and corresponding write data are output from a controller *after* the read command are output from the controller. In the Zumkehr system, when a read command is issued to the memory system before a write command and corresponding write data are issued to the memory system, the controller 210 defers the transfer of the write data from the controller 210 to the translator hub 220 until the read latency is met. *Zumkehr*

specification, column 7, lines 15-20 and Figure 5B. The disclosed system, however, does not require that the read latency be met before transferring the write command and corresponding write data from the controller to the memory system. Rather, the write command and corresponding write data may be provided to the memory system after the read command is issued to the memory system. This means that read data will be going in one direction to the controller and write data will be going in the opposite direction to a memory device at the same time. In order to prevent a collision on the data bus, the write data is decoupled from the bidirectional data bus by the bypass register. Once the read data has passed the bypass register, the write data is recoupled to the bidirectional data bus. Because the Zumkehr patent requires the write data to be already stored in the hub before a read command is issued, it does not meet all of the requirements for the method claims in the present application.

The Applicants propose canceling the apparatus claims, 1-4, 11-15, and 21-25 in the present application. The Applicants further propose filing a continuation application to prosecute amended apparatus claims separately from the method claims of the current application. In addition, the Applicants propose amending independent method claim 32 in the present application so that it has limitations similar to those already included in independent method claims 36 and 40, that the read command is issued to the memory system before the write data is provided to the memory system.

Upon the Examiner's acceptance of the proposed changes, all of the claims remaining in the application are clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,
DORSEY & WHITNEY LLP

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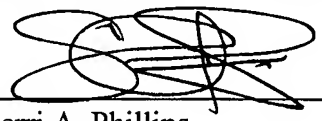
RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE - EXAMINING GROUP 2100

PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

June 5, 2007 

Date Sherri A. Phillips

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 10/773,583	Confirmation No.	: 6732
Applicants	: Douglas A. Larson and Jeffrey J. Cronin		
Filed	: February 5, 2004	Attorney Docket No.:	501296.01 (30266/US)
Art Unit	: 2188	Customer No.	: 27,076
Examiner	: Duc T. Doan		
Title	: APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM		

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Alexandria, VA 22313-1450

SUPPLEMENTAL RESPONSE UNDER 37 C.F.R. § 1.116

Sir:

Applicants acknowledge receipt of the Office Action dated December 5, 2006. Further to the response filed February 7, 2007, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 4 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 32-39.

Listing of Claims:

1-39. (Canceled)

40. (Previously Presented) A method for executing read and write commands in a memory system having a bidirectional memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system;

retrieving read data from the first memory location;

prior to receiving the read data on the memory bus from the memory system, providing write data corresponding to the write command to the bidirectional memory bus of the memory system;

in the memory system, bypassing the read data on the bidirectional memory bus;

receiving the read data on the bidirectional memory bus from the memory system; and

providing the write data to the bidirectional memory bus.

41. (Original) The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. (Original) The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. (Original) The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

REMARKS

Applicants filed a Notice of Appeal on April 5, 2007. Applicants acknowledge receipt of the Office Action dated December 5, 2006, and further to the response filed February 7, 2007, request the cancellation of claims 32-39.

Respectfully submitted,
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Enclosures:
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APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM

TECHNICAL FIELD

The present invention relates to memory systems, and more particularly, to memory modules having a data bypass for preventing data collision on a bi-direction data bus.

BACKGROUND OF THE INVENTION

Computer systems use memory devices, such as dynamic random access memory ("DRAM") devices, to store data that are accessed by a processor. These memory devices are normally used as system memory in a computer system. In a typical computer system, the processor communicates with the system memory through a processor bus and a memory controller. The memory devices of the system memory, typically arranged in memory modules having multiple memory devices, are coupled through a memory bus to the memory controller. The processor issues a memory request, which includes a memory command, such as a read command, and an address designating the location from which data or instructions are to be read. The memory controller uses the command and address to generate appropriate command signals as well as row and column addresses, which are applied to the system memory through the memory bus. In response to the commands and addresses, data are transferred between the system memory and the processor. The memory controller is often part of a system controller, which also includes bus bridge circuitry for coupling the processor bus to an expansion bus, such as a PCI bus.

In memory systems, high data bandwidth is desirable. Generally, bandwidth limitations are not related to the memory controllers since the memory controllers sequence data to and from the system memory as fast as the memory devices allow. One approach that has been taken to increase bandwidth is to increase the speed of the memory data bus coupling the memory controller to the memory devices. Thus, the same amount of

information can be moved over the memory data bus in less time. However, despite increasing memory data bus speeds, a corresponding increase in bandwidth does not result. One reason for the non-linear relationship between data bus speed and bandwidth is the hardware limitations within the memory devices themselves. That is, the memory controller has to schedule all memory commands to the memory devices such that the hardware limitations are honored. Although these hardware limitations can be reduced to some degree through the design of the memory device, a compromise must be made because reducing the hardware limitations typically adds cost, power, and/or size to the memory devices, all of which are undesirable alternatives. Thus, given these constraints, although it is easy for memory devices to move "well-behaved" traffic at ever increasing rates, for example, sequel traffic to the same page of a memory device, it is much more difficult for the memory devices to resolve "badly-behaved traffic," such as bouncing between different pages or banks of the memory device. As a result, the increase in memory data bus bandwidth does not yield a corresponding increase in information bandwidth.

In addition to the limited bandwidth between processors and memory devices, the performance of computer systems is also limited by latency problems that increase the time required to read data from system memory devices. More specifically, when a memory device read command is coupled to a system memory device, such as a synchronous DRAM ("SDRAM") device, the read data are output from the SDRAM device only after a delay of several clock periods. Therefore, although SDRAM devices can synchronously output burst data at a high data rate, the delay in initially providing the data can significantly slow the operating speed of a computer system using such SDRAM devices. Increasing the memory data bus speed can be used to help alleviate the latency issue. However, as with bandwidth, the increase in memory data bus speeds do not yield a linear reduction of latency, for essentially the same reasons previously discussed.

Although increasing memory data bus speed has, to some degree, been successful in increasing bandwidth and reducing latency, other issues are raised by this

approach. For example, as the speed of the memory data bus increases, loading on the memory bus needs to be decreased in order to maintain signal integrity since traditionally, there has only been wire between the memory controller and the memory slots into which the memory modules are plugged. Several approaches have been taken to accommodate the increase in memory data bus speed. For example, reducing the number of memory slots, adding buffer circuits on a memory module in order to provide sufficient fanout of control signals to the memory devices on the memory module, and providing multiple memory device interfaces on the memory module since there are too few memory module connectors on a single memory device interface. The effectiveness of these conventional approaches are, however, limited. A reason why these techniques were used in the past is that it was cost-effective to do so. However, when only one memory module can be plugged in per interface, it becomes too costly to add a separate memory interface for each required memory slot. In other words, it pushes the system controllers package out of the commodity range and into the boutique range, thereby, greatly adding cost.

One recent approach that allows for increased memory data bus speed in a cost effective manner is the use of multiple memory devices coupled to the processor through a memory hub. In a memory hub architecture, or a hub-based memory sub-system, a system controller or memory controller is coupled over a high speed bi-directional or unidirectional memory controller/hub interface to several memory modules. Typically, the memory modules are coupled in a point-to-point or daisy chain architecture such that the memory modules are connected one to another in series. Thus, the memory controller is coupled to a first memory module, with the first memory module connected to a second memory module, and the second memory module coupled to a third memory module, and so on in a daisy chain fashion.

Each memory module includes a memory hub that is coupled to the memory controller/hub interface and a number of memory devices on the module, with the memory hubs efficiently routing memory requests and responses between the controller and the memory devices over the memory controller/hub interface. Computer systems employing

this architecture can use a high-speed memory data bus since signal integrity can be maintained on the memory data bus. Moreover, this architecture also provides for easy expansion of the system memory without concern for degradation in signal quality as more memory modules are added, such as occurs in conventional memory bus architectures.

Although computer systems using memory hubs may provide superior performance, they may often fail to operate at optimum efficiency for a variety of reasons. One such reason is the issue of managing data collision between data flowing to and from the memory controller through the memory hubs. In conventional memory controllers, one approach taken to avoid data collision is to delay the execution of one memory command until the completion of another memory command. For example, with a conventional memory controller, a write command issued after a read command is not allowed to begin until the read command is nearly completed in order to avoid the read (i.e., inbound) data colliding with the write (i.e., outbound) data on the memory bus. However, forcing the write command to wait effectively reduces bandwidth, which is inconsistent with what is typically desired in a memory system.

SUMMARY OF THE INVENTION

One aspect of the present invention is directed to a memory hub having a data bypass circuit. The memory hub includes first and second link interfaces for coupling to respective data busses, a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces. The memory hub further includes a write bypass circuit coupled to the data path for coupling write data on the data path and temporarily storing the write data to allow read data to be transferred through the data path while the write data is temporarily stored. In another aspect of the invention, a method for writing data to a memory location in a memory system coupled to a memory bus is provided. The method includes accessing read data in the memory system, providing write data to the memory system on the memory bus, and coupling the write data to a register for temporary storage of the write data. While the data is temporarily stored,

the read data is coupled from the memory bus and provided for reading. The write data is recoupled to the memory bus and written to the memory location.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a computer system having memory modules in a memory hub architecture in which embodiments of the present invention can be implemented.

Figure 2 is a partial block diagram of a memory hub according to an embodiment of the present invention for use with the memory modules of Figure 1.

Figure 3 is a block diagram of a data bypass circuit for the memory hub of Figure 2 according to an embodiment of the present invention.

Figure 4 is a block diagram illustrating the operation of the data bypass circuit of Figure 3 for a computer system having the memory hub architecture of Figure 1 and the memory hub of Figure 2.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention are directed to a memory hub having bypass circuitry that provides data bypass for a bi-directional data bus in a hub-based memory sub-system. Certain details are set forth below to provide a sufficient understanding of various embodiments of the invention. However, it will be clear to one skilled in the art that the invention may be practiced without these particular details. In other instances, well-known circuits, control signals, and timing protocols have not been shown in detail in order to avoid unnecessarily obscuring the invention.

Figure 1 illustrates a computer system 100 according to one embodiment of the present invention. The computer system 100 includes a processor 104 for performing various computing functions, such as executing specific software to perform specific calculations or tasks. The processor 104 includes a processor bus 106 that normally includes an address bus, a control bus, and a data bus. The processor bus 106 is typically

coupled to cache memory 108. Typically, the cache memory 108 is provided by a static random access memory ("SRAM"). The processor bus 106 is also coupled to a system controller 110, which is sometimes referred to as a bus bridge.

The system controller 110 serves as a communications path to the processor 104 for a variety of other components. For example, as shown in Figure 1, the system controller 110 includes a graphics port that is typically coupled to a graphics controller 112. The graphics controller is typically coupled to a video terminal 114, such as a video display. The system controller 110 is also coupled to one or more input devices 118, such as a keyboard or a mouse, to allow an operator to interface with the computer system 100. Typically, the computer system 100 also includes one or more output devices 120, such as a printer, coupled to the processor 104 through the system controller 110. One or more data storage devices 124 are also typically coupled to the processor 104 through the system controller 110 to allow the processor 104 to store data or retrieve data from internal or external storage media (not shown). Examples of typical storage devices 124 include hard and floppy disks, tape cassettes, and compact disk read-only memories (CD-ROMs).

The system controller 110 includes a memory hub controller 128 that is coupled to memory hubs 140 of several memory modules 130a, 130b, 130c, . . . 130n. The memory modules 130 serve as system memory for the computer system 100, and are preferably coupled to the memory hub controller 128 through a high-speed bi-directional memory controller/hub interface 134. The memory modules 130 are shown coupled to the memory hub controller 128 in a point-to-point arrangement in which the memory controller/hub interface 134 is coupled through the memory hubs 140 of the memory modules 130. That is, the memory controller/hub interface 134 is a bi-directional bus that couples the memory hubs 140 in series. Thus, information on the memory controller/hub interface 134 must travel through the memory hubs 140 of "upstream" memory modules 130 to reach a "downstream" destination. For example, with specific reference to Figure 1, information transmitted from the memory hub controller 128 to the memory hub 140 of the

memory module 130c will pass through the memory hubs 140 of the memory modules 130a and 130b.

It will be appreciated, however, that topologies other than the point-to-point arrangement of Figure 1 may also be used. For example, a coupling arrangement may be used in which a separate high-speed link (not shown) is used to couple each of the memory modules 130 to the memory hub controller 128. A switching topology may also be used in which the memory hub controller 128 is selectively coupled to each of the memory modules 130 through a switch (not shown). Other topologies that may be used will be apparent to one skilled in the art. Additionally, the memory controller/hub interface 134 coupling the memory modules to the memory hub controller may be an electrical or optical communication path. However, other types of communications paths can be used for the memory controller/hub interface 134 as well. In the event the memory controller/hub interface 134 is implemented as an optical communication path, the optical communication path may be in the form of one or more optical fibers. In such case, the memory hub controller 128 and the memory modules will include an optical input/output port or separate input and output ports coupled to the optical communication path, as well known in the art.

The memory hubs 140 control access to memory devices 148 of the respective memory module 130. In Figure 1, the memory devices are illustrated as synchronous dynamic random access memory ("SDRAM") devices. However, memory devices other than SDRAM devices may also be used. As also shown in Figure 1, the memory hub is coupled to four sets of memory devices 148 through a respective memory bus 150. Each of the sets includes four memory devices 148 for a total of 20 memory devices 148 for each memory module 130. The memory busses 150 normally include a control bus, an address bus, and a data bus, as known in the art. However, it will be appreciated by those ordinarily skilled in the art that other bus systems, such as a bus system using a shared command/address bus, may also be used without departing from the scope of the present invention. It will be further appreciated that the arrangement of the

memory devices 148, and the number of memory devices 148 can be modified without departing from the scope of the present invention.

Figure 2 illustrates a portion of the memory hub 140 according to an embodiment of the present invention. The memory hub 140 includes a local hub circuit 214 coupled to the memory controller/hub interface 134 (Figure 1). The local hub circuit 214 is further coupled to memory devices 148 through the memory bus 150. The local hub circuit 214 includes control logic for processing memory commands issued from the memory controller 128 and for accessing the memory devices 148 over the memory bus 150 to provide the corresponding data when the memory command is directed to the respective memory module 130. The design and operation of such control logic is well known by those ordinarily skilled in the art, and consequently, a more detailed description has been omitted from herein in the interest of brevity. The memory hub 140 further includes a data bypass circuit 286 coupled to the local hub circuit 214. As will be explained in more detail below, the data bypass circuit 286 is used to temporarily capture data passing to a distant memory hub, which allows data returning from another distant memory hub to pass through the memory hub 140 before the captured data continues onto the distant memory hub. Thus, the data bypass circuit 286 provides a data bypass mechanism that can be used to avoid data collisions on the bi-directional memory controller/hub interface 134 to which the memory hub 140 is coupled.

As previously discussed, one approach taken by conventional memory sub-systems to avoid data collision is to delay the execution of one memory command until the completion of another memory command. For example, in typical memory systems a write command issued after a read command would not have been allowed to start until near the completion of the read command in order to avoid the read (i.e., inbound) data colliding with the write (i.e., outbound) data on the memory controller/hub interface 134. In contrast, by employing the memory hub 140 having the data bypass circuit 286, write commands issued after a read command can be sequenced earlier than compared with

conventional memory systems, and consequently, memory commands scheduled after the earlier scheduled write command can be executed sooner as well. .

Figure 3 illustrates a data bypass circuit 300 according to an embodiment of the present invention. The data bypass circuit 300 can be substituted for the data bypass circuit 286 (Figure 2) and can be implemented using conventional designs and circuits well known to those ordinarily skilled in the art. The data bypass circuit 300 includes an input buffer 302 that receives input write data WR-DATA_IN and provides the same to a bypass register/FIFO 304 and a first input of a multiplexer 306. An output of the bypass register/FIFO 304 is coupled to a second input of the multiplexer 306. Selection of which of the two inputs to couple to the output of the multiplexer 306 is made by an enable signal EN generated by a bypass select logic 308. The EN signal is also provided to an input/output buffer 310 as an output enable signal activating or deactivating the input/output buffer 310. The bypass select logic 308 generates the appropriate EN signal in response to an activation signal BYPASS_EN provided by the memory hub controller 128 (Figure 1). Alternatively, the BYPASS_EN signal may be provided from other memory hubs (not shown) that are part of the same memory system. The circuitry of the data bypass circuit is conventional, and it will be appreciated that the circuits of the data bypass circuit 300 can be implemented using conventional designs and circuitry well known in the art.

In operation, WR_DATA_IN received by the data bypass circuit 300 is driven through the input buffer 302 and is provided to the first input of the multiplexer 306. The WR_DATA_IN is also saved in the bypass register/FIFO 304. In response to an inactive BYPASS_EN signal, an active EN signal is generated by the bypass select logic 308. The active EN signal enables output by the input/output buffer 310 and couples the output of the input buffer 302 to the input of the input/output buffer 310 through the multiplexer 306. As a result, the WR_DATA_IN is provided directly to the input of the input/output buffer 310 and the WR_DATA_IN is provided through the data bypass circuit 300 without any bypass. However, in response to an active BYPASS_EN signal, the bypass select logic 308 generates an inactive EN signal, disabling the output function of the

input/output buffer 310 and placing its output in a high-impedance state. Additionally, the inactive EN signal couples the input of the input/output buffer 310 to the output of the bypass register/FIFO 304. In this manner, the WR_DATA_IN is received by the data bypass circuit 300, stored by the bypass register/FIFO 306, and applied to the input of the input/output buffer 310. However, due to the inactive state of the EN signal, the WR_DATA_IN is not provided as output data WR_DATA_OUT by the input/output buffer 310. As a result, the WR_DATA_IN is held in a bypass state until the BYPASS_EN signal becomes inactive, at which time, the EN signal become active again, enabling the input/output buffer 310 to provide the WR_DATA_IN as WR_DATA_OUT data. The multiplexer 306 is also switched back to coupling the output of the input buffer 302 directly to the input of the input/output buffer 310 to allow WR_DATA_IN to pass through the data bypass circuit unhindered.

Operation of the data bypass circuit 286 will be described with reference to Figure 4. Figure 4 is similar to Figure 1, except that Figure 4 has been simplified. In particular, many of the functional blocks of Figure 1 have been omitted, with only the memory modules 130a-130c being shown, and represented by memory hubs 140a-140c. Only one memory device 148a-148c is shown to be coupled to a respective memory hub 140a-140c through a respective memory bus 150a-150c. As with Figure 1, the memory hubs 140a-140c are coupled by a high-speed bi-directional memory controller/hub interface 134 to a memory hub controller 128.

In Figure 4, it is assumed that the memory hub controller 128 has just issued read and write commands, with the read command sequenced prior to the write command. The read command is directed to the memory module 130b and the write command is directed to the memory module 130c. That is, the memory module to which data will be written is further downstream than the memory module from which data is read. In response to the read command, the memory hub 140b begins retrieving the read data (RD) from the memory device 148b, as indicated in Figure 4 by the "(1)". With the read command issued, the write command is then initiated, and the write data (WD) is provided

onto the memory controller/hub interface 134. However, since the memory hub controller 128 is expecting the RD to be returned from the memory module 130b, the memory hub 140a is directed to capture the WD in its data bypass circuit 286a. As a result, the memory hub 286a captures the WD to clear the memory controller/hub interface 134, as indicated in Figure 4 by the "(2)", for the RD to be returned to the memory hub controller 128. When the memory hub 140b has retrieved the RD from the memory device 148b, the RD is then provided to the memory hub controller 128 through the memory controller/hub interface 134, as indicated in Figure 4 by the "(3)" to complete the read request. Upon the RD passing through the memory hub 140a on its way to the memory hub controller 128, the memory hub 140a releases the WD from the data bypass circuit 286a to continue its way to the memory hub 140c. The WD is provided to the memory hub 140c through the high-speed link, which is now clear between the memory hub 140a and 140c. Upon reaching the memory hub 140c, the WD is written in the memory device 148c, as shown in Figure 4 by the "(4)". In an embodiment of the present invention, coordination of the data flow of the RD and WD on the memory controller/hub interface 134 and through the data bypass circuits 286 is under the control of the memory hub controller 128. For example, in the previous example the memory hub controller ensures that any WD flowing in the opposite direction of the RD is out of the way when retrieving RD from the memory module 130b. It will be appreciated, however, that in alternative embodiments data flow through the memory controller/hub interface 134 and the data bypass circuits 286 can be managed differently, such as the memory hub controller 128 sharing coordination of the data flow with the memory hubs 140.

In the previous example, the RD is returned to the memory hub controller 128 as in a conventional memory system. That is, the RD transmitted by the memory devices 148 is provided to the memory controller without any significant delay. However, by employing the previously described data bypass mechanism, write commands can be scheduled earlier than with conventional memory systems. A write command issued after a read command would not have been allowed to start until near the completion of the read

command in typical memory systems. In contrast, embodiments of the present invention allow a subsequently issued write command to be scheduled earlier, thus, reducing the time gap between read and write commands. As a result, commands scheduled behind an earlier scheduled write command have an overall reduced latency.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

1. A memory hub for a hub-based memory module, comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

2. The memory hub of claim 1 wherein the write bypass circuit comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

3. The memory hub of claim 2 wherein the write bypass circuit further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

4. The memory hub of claim 1, further comprising a memory device interface coupled to the data path, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

5. A memory hub for a hub-based memory module, comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

6. The memory hub of claim 5 wherein the data bypass circuit comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

7. The memory hub of claim 6 wherein the data bypass circuit further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

8. The memory hub of claim 5, further comprising a memory device interface coupled to the switching circuit, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

9. The memory hub of claim 8 wherein the memory device interface comprises:

a memory controller coupled to the data path through a memory controller bus and further having a memory device terminal to which a memory device can be coupled;

a write buffer coupled to the memory controller for storing memory requests; and

a cache coupled to the memory controller for storing data.

10. The memory hub of claim 5 wherein the first set of data represents write data and the second set of data represents read data.

11. A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, the memory hub comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

12. The memory module of claim 11 wherein the write bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

13. The memory module of claim 12 wherein the write bypass circuit of the memory hub further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

14. The memory module of claim 11 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

15. The memory module of claim 14 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

16. A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to at least one of the plurality of memory devices, the memory hub comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

17. The memory module of claim 16 wherein the data bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer

input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

18. The memory module of claim 17 wherein the data bypass circuit of the memory hub further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

19. The memory module of claim 16 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

20. The memory module of claim 16 wherein the first set of data represents write data and the second set of data represents read data.

21. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the plurality of memory devices, the memory hub comprising:

first and second link interfaces for coupling to respective data busses;

a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces; and

a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored.

22. The processor-based system of claim 21 wherein the write bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

23. The processor-based system of claim 22 wherein the write bypass circuit of the memory hub further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register.

24. The processor-based system of claim 21 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

25. The processor-based system of claim 24 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

26. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a system memory port and a peripheral device port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

a plurality of memory devices; and

a memory hub coupled to at least one of the plurality of memory devices, the memory hub comprising:

a first link interface for coupling to a first data bus to provide data to the first data bus and receive data from the first data bus;

a second link interface for coupling to a second data bus to provided data to the second data bus and receive data from the second data bus;

a switching circuit coupled to the first and second link interfaces to couple data between the first and second link interfaces; and

a data bypass circuit coupled to the switching circuit to store a first set of data received by either the first or second link interfaces to allow a second set of data to be coupled between the first and second link interfaces without interference by the first set of data.

27. The processor-based system of claim 26 wherein the data bypass circuit of the memory hub comprises:

a multiplexer having a first input coupled to the switching circuit and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal;

a first-in-first-out (FIFO) register having an input coupled to the switching circuit and further having an output coupled to the second input of the multiplexer;

an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and

a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer.

28. The processor-based system of claim 27 wherein the data bypass circuit of the memory hub further comprises an input buffer having an input coupled to the switching circuit and an output coupled to the inputs of the multiplexer and the FIFO register.

29. The processor-based system of claim 26 wherein the memory hub further comprises a memory device interface coupled to the data path and to at least one of the plurality of memory devices, the memory device interface for coupling data to the memory device.

30. The processor-based system of claim 29 wherein the memory device interface of the memory hub comprises:

a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus;

a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and

a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device.

31. The processor-based system of claim 26 wherein the first set of data represents write data and the second set of data represents read data.

32. A method for writing data to a memory location in a memory system coupled to a memory bus, comprising:

accessing read data in the memory system;

providing write data to the memory system on the memory bus;

coupling the write data to a register in the memory system for temporary storage of the write data;

coupling the read data to the memory bus and providing the read data for reading;

coupling the write data stored in the register to the memory bus; and

writing the write data to the memory location.

33. The method of claim 32, further comprising issuing a read command to the memory system prior to issuing a write command to the memory system.

34. The method of claim 32 wherein providing the write data to the memory system comprises providing the write data through at least one memory module of the memory system prior to coupling the write data to the register.

35. The method of claim 32 wherein the memory system includes a plurality of memory modules coupled in series on the memory bus, and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed.

36. A method for executing memory commands in a memory system having a memory bus, the method comprising:

issuing a read command to the memory system;

issuing a write command to a memory location in the memory system and providing write data to the memory bus of the memory system;

accessing read data in the memory system;

in the memory system, decoupling the write data from the memory bus;

receiving the read data on the memory bus from the memory system;

recoupling the write data to the memory bus; and

resuming the write command to the memory location.

37. The method of claim 36 wherein issuing the read command to the memory system precedes issuing the write command to the memory system.

38. The method of claim 36, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

39. The method of claim 36 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

40. A method for executing read and write commands in a memory system having a memory bus, the method comprising:

issuing a read command to access a first memory location in the memory system;

before completion of the read command, scheduling a write command to write data to a second memory location in the memory system

retrieving read data from the first memory location;

providing write data to the memory bus of the memory system;

in the memory system, bypassing the read data on the memory bus;

receiving the read data on the memory bus from the memory system; and

providing the write data to the memory bus.

41. The method of claim 40 wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus.

42. The method of claim 41, further comprising temporarily storing the write data in a bypass buffer during the receipt of the read data.

43. The method of claim 41 wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus.

APPARATUS AND METHOD FOR DATA BYPASS FOR A BI-DIRECTIONAL DATA BUS IN A HUB-BASED MEMORY SUB-SYSTEM

ABSTRACT OF THE DISCLOSURE

A memory hub includes first and second link interfaces for coupling to respective data busses, a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces, and further includes a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored. A method for writing data to a memory location in a memory system is provided which includes accessing read data in the memory system, providing write data to the memory system, and coupling the write data to a register for temporary storage. The write data is recoupled to the memory bus and written to the memory location following provision of the read data.

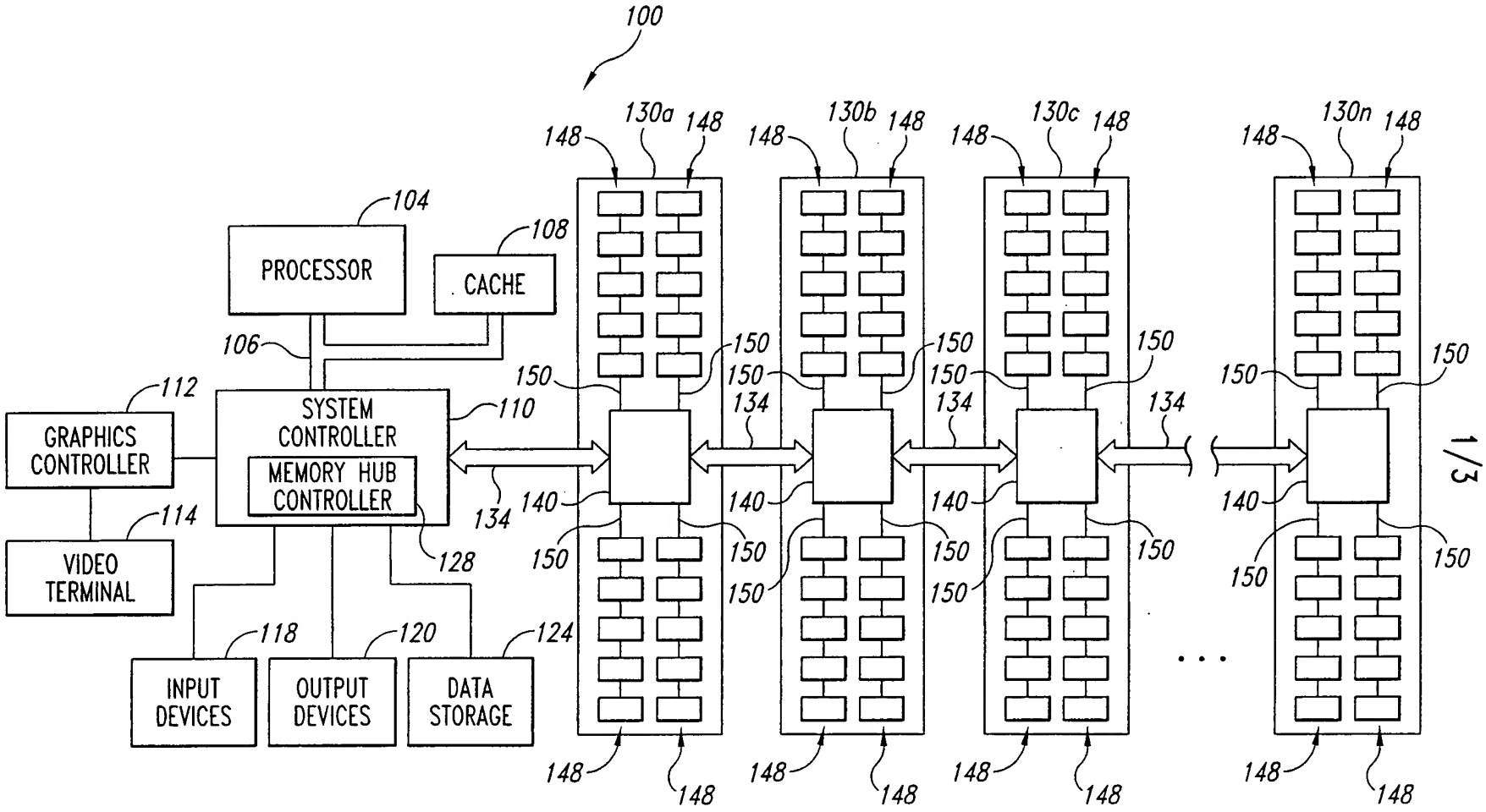
100
PROCESSOR
104
CACHE
108
106
GRAPHICS CONTROLLER
112
SYSTEM CONTROLLER
110
MEMORY HUB CONTROLLER
128
VIDEO TERMINAL
114
INPUT DEVICES
118
OUTPUT DEVICES
120
DATA STORAGE
124
130a
130b
130c
130n
148
150
134
140

Fig. 1

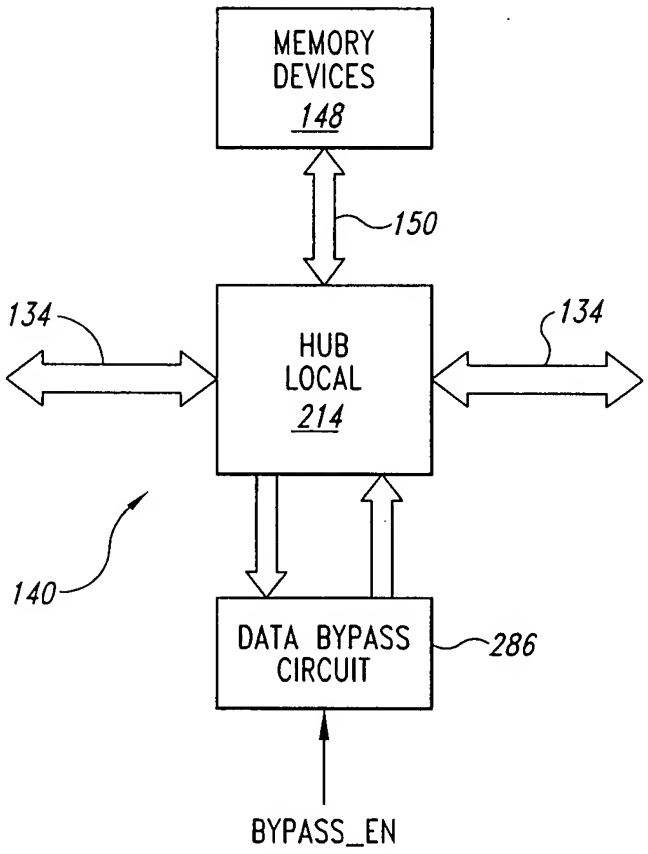
MEMORY
DEVICES
148
150
134
134
HUB
LOCAL
214
140
DATA BYPASS
CIRCUIT
286
BYPASS_EN

Fig. 2

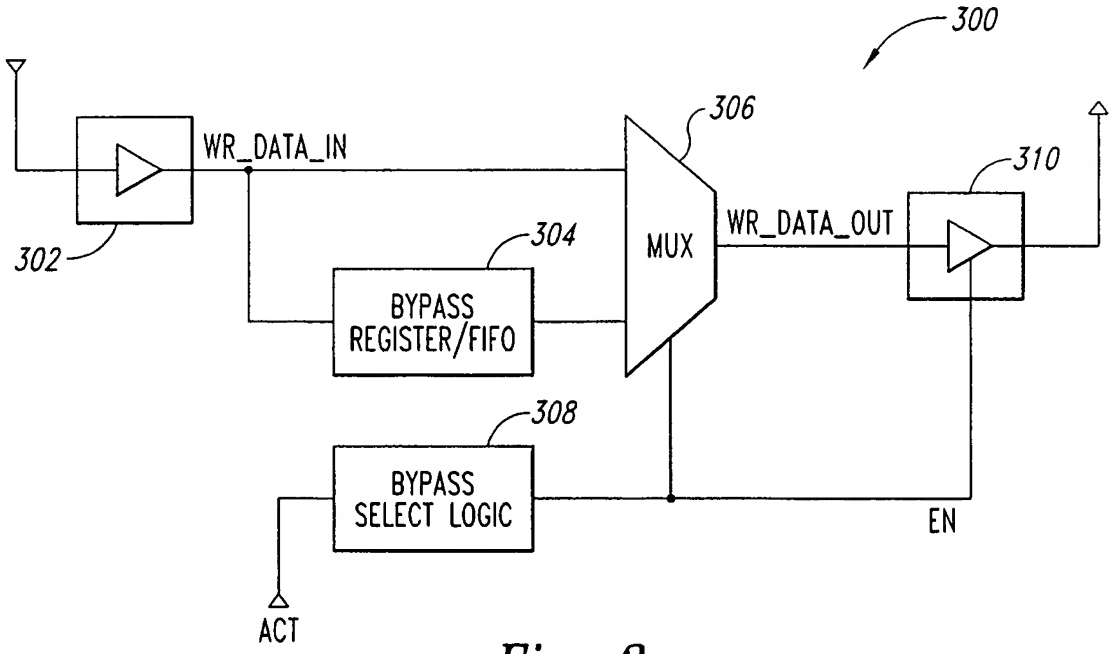
300
306
310
WR_DATA_IN
WR_DATA_OUT
MUX
302
304
BYPASS
REGISTER/FIFO
308
BYPASS
SELECT LOGIC
EN
ACT

Fig. 3

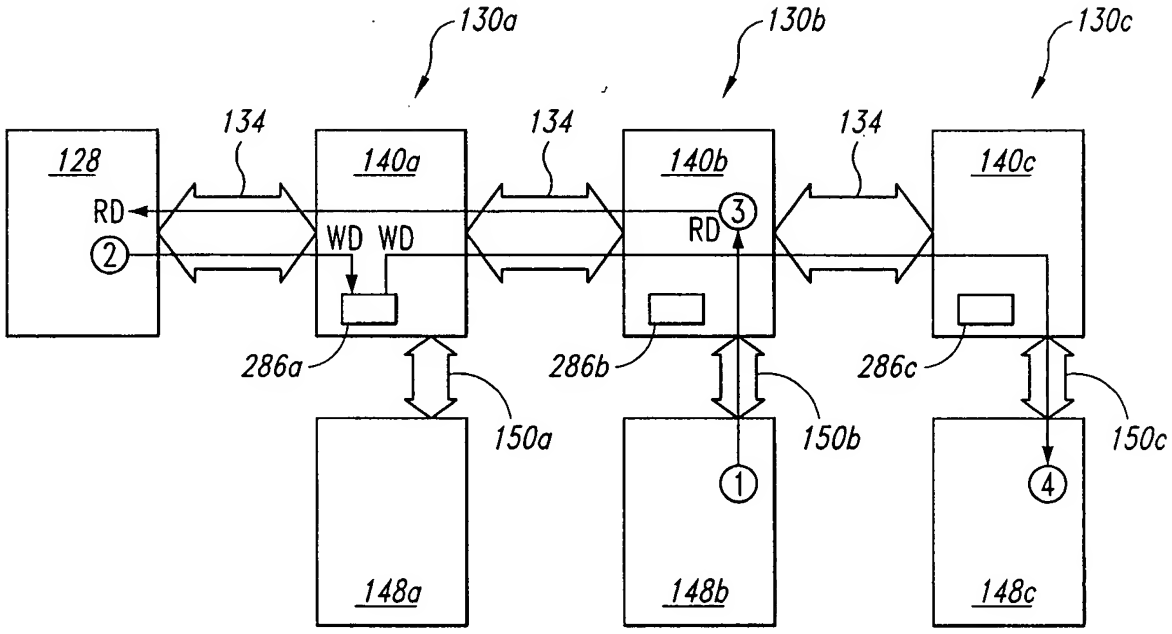
130a
130b
130c
134
134
134
128
140a
140b
140c
RD
WD WD
RD
2
3
286a
286b
286c
150a
150b
150c
1
4
148a
148b
148c

Fig. 4